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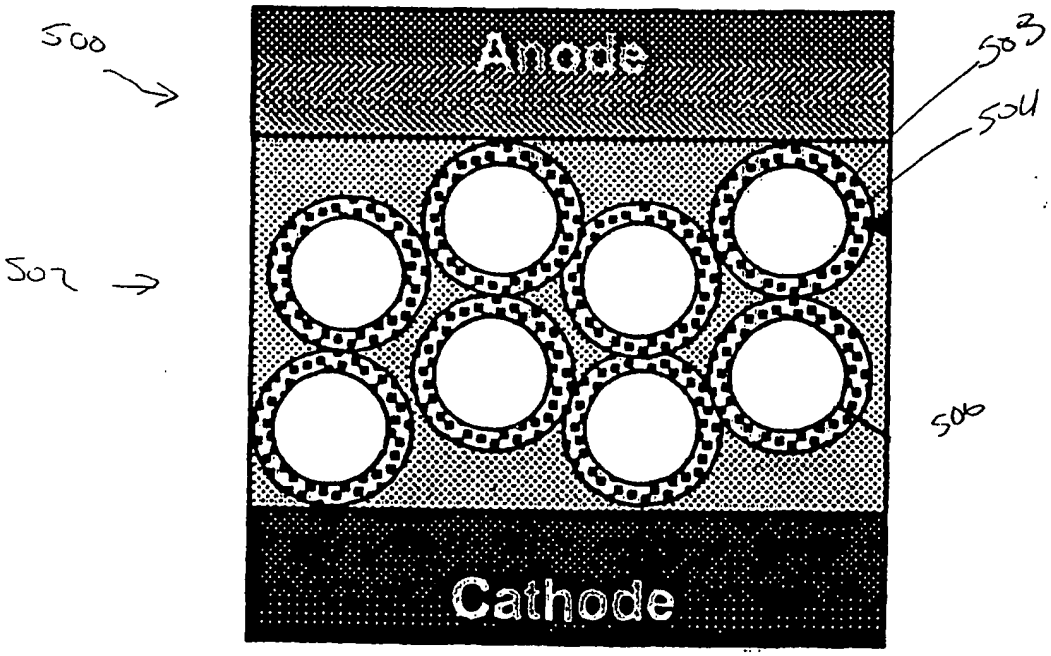
(54) Title: PROGRAMMABLE MICROELECTRONIC DEVICE, STRUCTURE, AND SYSTEM, AND METHOD OF FORMING THE SAME




(57) Abstract: A microelectronic programmable structure suitable for storing information and a method of forming and programming the structure are disclosed. The programmable structure generally includes an ion conductor and a plurality of electrodes. Electrical properties of the structure may be altered by applying energy to the structure, and thus information may be stored using the structure.

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# PROGRAMMABLE MICROELECTRONIC DEVICE, STRUCTURE, AND SYSTEM AND METHOD OF FORMING THE SAME

## 1. Field of Invention

The present invention generally relates to programmable microelectronic devices. More particularly, the invention relates to programmable microelectronic structures and devices having an electrical property that can be variably programmed by manipulating an amount of energy supplied to the structure during a programming function.

## 2. Background of the Invention

Memory devices are often used in electronic systems and computers to store information in the form of binary data. These memory devices may be characterized into various types, each type having associated with it various advantages and disadvantages.

For example, random access memory ("RAM"), which may be found in personal computers, is typically volatile semiconductor memory; in other words, the stored data is lost if the power source is disconnected or removed. Dynamic RAM ("DRAM") is particularly volatile in that it must be "refreshed" (*i.e.*, recharged) every few hundred milliseconds in order to maintain the stored data. Static RAM ("SRAM") will hold the data after one writing so long as the power source is maintained; once the power source is disconnected, however, the data is lost. Thus, in these volatile memory configurations, information is only retained so long as the power to the system is not turned off. In general, these RAM devices can take up significant chip area and therefore may be expensive to manufacture and consume relatively large amounts of energy for data storage. Accordingly, improved memory devices suitable for use in personal computers and the like are desirable.

Other storage devices such as magnetic storage devices (*e.g.*, floppy disks, hard disks and magnetic tape) as well as other systems, such as optical disks, CD-RW and DVD-RW are non-volatile, have extremely high capacity, and can be rewritten many times. Unfortunately, these memory devices are physically large, are shock/vibration-sensitive, require expensive mechanical drives, and may consume relatively large amounts of power. These negative aspects make such memory devices non-ideal for low power portable applications such as lap-top and palm-top computers, personal digital assistants ("PDAs"), and the like.

Due, at least in part, to a rapidly growing numbers of compact, low-power portable computer systems and hand-held appliances in which stored information changes regularly, low energy read/write semiconductor memories have become increasingly desirable and widespread. Furthermore, because these portable systems often require data storage when the power is turned off, non-volatile storage device are desired for use in such systems.

One type of programmable semiconductor non-volatile memory device suitable for use in such systems is a programmable read-only memory ("PROM") device. One type of PROM, a write-once read-many ("WORM") device, uses an array of fusible links. Once programmed, the WORM device cannot be reprogrammed.

Other forms of PROM devices include erasable PROM ("EPROM") and electrically erasable PROM (EEPROM) devices, which are alterable after an initial programming. EPROM devices generally require an erase step involving exposure to ultra violet light prior to programming the device. Thus, such devices are generally not well suited for use in portable electronic devices. EEPROM devices are generally easier to program, but suffer from other deficiencies. In particular, EEPROM devices are relatively complex, are relatively difficult to manufacture, and are relatively large. Furthermore, a circuit including EEPROM devices must withstand the high voltages necessary to program the device. Consequently, EEPROM cost per bit of memory capacity is extremely high compared with other means of data storage. Another disadvantage of EEPROM devices is that, although they can retain data without having the power source connected, they require relatively large amounts of power to program. This power drain can be considerable in a compact portable system powered by a battery.

Various hand-held appliances such as PDAs, portable phones, and the like as well as other electronic systems generally include a memory device coupled to a microprocessor and/or microcontroller formed on a separate substrate. For example, portable computing systems include a microprocessor and one or more memory chips coupled to a printed circuit board.

Forming memory devices and the microprocessor on separate substrates may be undesirable for several reasons. For example, forming various types of memory on separate substrate may be relatively expensive, may require relatively long transmission paths to communicate between the memory devices and any associated electronic device, and may require a relatively large amount of room within a system. Accordingly, memory structures that may be formed on the same substrate as another electronic device and methods of

forming the same are desired. Furthermore, this memory technology desirably operates at a relatively low voltage while providing high speed memory with high storage density and a low manufacturing cost.

## SUMMARY OF THE INVENTION

The present invention provides improved microelectronic programmable devices, structures, and systems and methods of forming the same. More particularly, the invention provides programmable structures that can be variably programmed depending on an amount of energy used to program the device. Such structures can replace both traditional nonvolatile and volatile forms of memory and can be formed on the same substrate and/or overlying another microelectronic device.

The ways in which the present invention addresses various drawbacks of now-known programmable devices are discussed in greater detail below. However, in general, the present invention provides a programmable device that is relatively easy and inexpensive to manufacture, which is relatively easy to program, and which can be variably programmed.

In accordance with one exemplary embodiment of the present invention, a programmable structure includes an ion conductor and at least two electrodes. The structure is configured such that when a bias is applied across two electrodes, one or more electrical properties of the structure change. In accordance with one aspect of this embodiment, a resistance across the structure changes when a bias is applied across the electrodes. In accordance with other aspects of this embodiment, a capacitance or other electrical property of the structure changes upon application of a bias across the electrodes. In accordance with a further aspect of this embodiment, an amount of change in the programmable property is manipulated by altering (e.g., thermally or electrically) an amount of energy used to program the device. One or more of these electrical changes and/or the amount of change may suitably be detected. Thus, stored information may be retrieved from a circuit including the structure.

In accordance with another exemplary embodiment of the invention, a programmable structure includes an ion conductor, at least two electrodes, and a barrier interposed between at least a portion of one of the electrodes and the ion conductor. In accordance with one aspect of this embodiment, the barrier material includes a material configured to reduce diffusion of ions between the ion conductor and at least one electrode. In accordance with another aspect, the barrier material includes an insulating or high-resistance material. In

accordance with yet another aspect of this embodiment, the barrier includes material that conducts ions, but which is relatively resistant to the conduction of electrons.

In accordance with another exemplary embodiment of the invention, a programmable microelectronic structure is formed on a surface of a substrate by forming a first electrode on the substrate, depositing a layer of ion conductor material over the first electrode, and depositing conductive material onto the ion conductor material. In accordance with one aspect of this embodiment, a solid solution including the ion conductor and excess conductive material is formed by dissolving (*e.g.*, via thermal and/or photodissolution) a portion of the conductive material in the ion conductor. In accordance with a further aspect, only a portion of the conductive material is dissolved, such that a portion of the conductive material remains on a surface of the ion conductor to form an electrode on a surface of the ion conductor material. In accordance with another aspect of this embodiment of the invention, a structure including a high-resistance region is formed by dissolving a portion of the electrode such that a portion of the ion conductor includes a high concentration of the electrode material and another portion of the ion conductor includes a low concentration of the electrode material, such that the portion of the ion conductor with a low concentration of the electrode material forms a high resistance region within the structure.

In accordance with another embodiment of the present invention, at least a portion of a programmable structure is formed within a through-hole or via in an insulating material. In accordance with one aspect of this embodiment, a first electrode feature is formed on a surface of a substrate, insulating material is deposited onto a surface of the electrode feature, a via is formed within the insulating material, and a portion of the programmable structure is formed within the via. After the via is formed within the insulating material, a portion of the structure within the via is formed by depositing an ion conductive material onto the conductive material, depositing a second electrode material onto the ion conductive material, and, if desired, removing any excess electrode, ion conductor, and/or insulating material. In accordance with another aspect of this embodiment, only the ion conductor is formed within the via. In this case, a first electrode is formed below the insulating material and in contact with the ion conductor and the second electrode is formed above the insulating material and in contact with the ion conductor. The configuration of the via may be changed to alter (e.g., reduce) a contact area between one or more of the electrodes and the ion conductor. Reducing the cross-sectional area of the interface between the ion conductor and the electrode increases the efficiency of the device (change in electrical property per amount of

power supplied to the device). In accordance with another aspect of this embodiment, the via may extend through the lower electrode to reduce the interface area between the electrode and the ion conductor. In accordance with yet another aspect of this embodiment, a portion of the ion conductor may be removed from the via or the ion conductor material may be directionally deposited into only a portion of the via to further reduce an interface between an electrode and the ion conductor.

In accordance with another embodiment of the invention, a programmable device may be formed on a surface of a substrate. In accordance with one aspect of this embodiment, the substrate includes a microelectronic circuit. In accordance with a further aspect of this embodiment, the memory device is formed overlying the microelectronic circuit and conductive lines between the microelectronic circuit and the memory are formed using conductive wiring schemes within the substrate and the memory device. This configuration allows transmission of more bits of information per bus line.

In accordance with a further exemplary embodiment of the invention, multiple bits of information are stored in a single programmable structure. In accordance with one aspect of this embodiment, a programmable structure includes a floating electrode interposed between two additional electrodes.

In accordance with yet another embodiment of the invention, multiple programmable devices are coupled together using a common electrode (e.g., a common anode or a common cathode).

In accordance with yet a further exemplary embodiment of the present invention, a capacitance of a programmable structure is altered by causing ions within an ion conductor of the structure to migrate.

In accordance with yet another embodiment of the invention, a volatility of a memory cell in accordance with the present invention is manipulated by altering an amount of energy used during a write process for the memory. In accordance with this embodiment of the invention, higher energy is used to form nonvolatile memory, while lower energy is used to form volatile memory. Thus, a single memory device, formed on a single substrate, may include both nonvolatile and volatile portions. In accordance with a further aspect of this embodiment, the relative volatility of one or more portions of the memory may be altered at any time by changing an amount of energy supplied to a portion of the memory during a write process.

## BRIEF DESCRIPTION OF THE DRAWINGS

A more complete understanding of the present invention may be derived by referring to the detailed description and claims, considered in connection with the figures, wherein like reference numbers refer to similar elements throughout the figures, and:

Figures 1 and 2 are cross-sectional illustrations of a programmable structure formed on a surface of a substrate in accordance with the present invention;

Figures 3-5 cross-sectional illustration of a programmable structure in accordance with another embodiment of the present invention. illustrating phase-separated ion conductors;

Figures 6-8 are current-voltage diagrams illustrating current and voltage characteristics of the devices of the present invention;

Figures 9-13 illustrate programmable structures including barrier layers in accordance with exemplary embodiments of the invention;

Figure 14 is a cross-sectional illustration of a programmable structure in accordance with yet another embodiment of the present invention;

Figure 15 and 16 are schematic illustrations of a portion of a memory device in accordance with an exemplary embodiment of the present invention;

Figures 17 and 18 are illustrations of programmable structures having an ion conductor/electrode contact interface formed about a perimeter of the ion conductor in accordance with another embodiment of the present invention;

Figures 19 and 20 are illustrations of programmable structures having an ion conductor/electrode contact interface formed about a perimeter of the ion conductor in accordance with yet another embodiment of the present invention;

Figures 21 and 22 illustrate a programmable device having a horizontal configuration in accordance with the present invention;

Figures 23-28 illustrate programmable device structures with reduced electrode/ion conductor interface surface area in accordance with the present invention;

Figure 29 illustrates a programmable device with a tapered ion conductor in accordance with the present invention;

Figures 30-33 illustrate a programmable device including a floating electrode in accordance with the present invention; and

Figures 34-38 illustrate common electrode programmable device structures in accordance with the present invention.

Skilled artisans will appreciate that elements in the figures are illustrated for simplicity and clarity and have not necessarily been drawn to scale. For example, the dimensions of some of the elements in the figures may be exaggerated relative to other elements to help to improve understanding of embodiments of the present invention.

## DETAILED DESCRIPTION

The present invention generally relates to programmable microelectronic devices, to systems including the devices, and to methods of forming the devices and systems.

Figures 1 and 2 illustrate programmable microelectronic structures 100 and 200 formed on a surface of a substrate 110 in accordance with an exemplary embodiment of the present invention. Structures 100 and 200 include electrodes 120 and 130, an ion conductor 140, and optionally include buffer or barrier layers or regions 155 and/or 255.

Generally, structures 100 and 200 are configured such that when a bias greater than a threshold voltage ($V_T$), discussed in more detail below, is applied across electrodes 120 and 130, the electrical properties of structure 100 change. For example, in accordance with one embodiment of the invention, as a voltage $V \geq V_T$ is applied across electrodes 120 and 130, conductive ions within ion conductor 140 begin to migrate and form a region 160 having an increased conductivity compared to the bulk ion conductor (*e.g.*, an electrodeposit) at or near the more negative of electrodes 120 and 130. As region 160 forms, the resistance between electrodes 120 and 130 decreases, and other electrical properties may also change. In the absence of any barriers, which are discussed in more detail below, the threshold voltage required to grow region 160 from one electrode toward the other and thereby significantly reduce the resistance of the device is approximately the reduction/oxidation potential of the system, typically a few hundred millivolts. If the same voltage is applied in reverse, region 160 will dissolve back into the ion conductor and the device will return to a high resistance state.

Structures 100 and 200 may be used to store information and thus may be used in memory circuits. For example, structure 100 or other programmable structures in accordance with the present invention may suitably be used in memory devices to replace DRAM, SRAM, PROM, EPROM, EEPROM devices, or any combination of such memory. In addition, programmable structures of the present invention may be used for other applications where programming or changing of electrical properties of a portion of an electrical circuit are desired.

In accordance with various embodiments of the invention, the volatility of programmable memory (e.g., cell 100 or 200) can be manipulated by altering an amount of energy (e.g., altering time, current, voltage, thermal energy, and/or the like) applied during a write process. In the case where region 160 forms during a write process, the greater the amount of energy (having a voltage greater than the threshold voltage for the write process) applied during the write process, the greater the growth of region 160 and hence the less volatile the memory. Conversely, relatively volatile easily erased memory can be formed by supplying relatively little energy to the cell. Thus, relatively volatile memory can be formed using the same or similar structures used to form nonvolatile memory, and less energy can be used to form the volatile/easily erased memory. Use of less energy is particularly desirable in portable electronic devices that depend on stored energy for operation. The volatile and nonvolatile memory may be formed on the same substrate and partitioned or separated from each other such that each partition is dedicated to either volatile or nonvolatile memory; or, an array of memory cells may be configured as volatile or nonvolatile memory using programming techniques, such that the configuration (i.e., volatile or nonvolatile) of the memory can be altered by changing an amount of energy supplied during programming the respective portions of the memory array.

Referring again to Figures 1 and 2, substrate 110 may include any suitable material. For example, substrate 110 may include semiconductive, conductive, semiinsulative, insulative material, or any combination of such materials. In accordance with one embodiment of the invention, substrate 110 includes an insulating material 112 and a portion 114 including a microelectronic devices formed using a portion of the substrate. Layer 112 and portion 114 may be separated by additional layers (not shown) such as, for example, layers typically used to form integrated circuits. Because the programmable structures can be formed over insulating or other materials, the programmable structures of the present invention are particularly well suited for applications where substrate (e.g., semiconductor material) space is a premium. In addition, forming a memory cell overlying a microelectronic device may be advantageous because such a configuration allows greater data transfer between an array of memory cells and the microelectronic device using, for example, conductive plugs formed within layers 112 and 150.

Electrodes 120 and 130 may be formed of any suitable conductive material. For example, electrodes 120 and 130 may be formed of doped polysilicon material or metal.

In accordance with one exemplary embodiment of the invention, one of electrodes 120 and 130 is formed of a material including a metal that dissolves in ion conductor 140 when a sufficient bias ($V \geq V_T$) is applied across the electrodes (an oxidizable electrode) and the other electrode is relatively inert and does not dissolve during operation of the programmable device (an indifferent electrode). For example, electrode 120 may be an anode during a write process and be comprised of a material including silver that dissolves in ion conductor 140 and electrode 130 may be a cathode during the write process and be comprised of an inert material such as tungsten, nickel, molybdenum, platinum, metal silicides, and the like. Having at least one electrode formed of a material including a metal which dissolves in ion conductor 140 facilitates maintaining a desired dissolved metal concentration within ion conductor 140, which in turn facilitates rapid and stable region 160 formation within ion conductor 140 or other electrical property change during use of structure 100 and/or 200. Furthermore, use of an inert material for the other electrode (cathode during a write operation) facilitates electrodissolution of any region 160 that may have formed and/or return of the programmable device to an erased state after application of a sufficient voltage.

During an erase operation, dissolution of any region 160 that may have formed preferably begins at or near the oxidizable electrode/region 160 interface. Initial dissolution of the region 160 at the oxidizable electrode/region 160 interface may be facilitated by forming structure 100 such that the resistance at the oxidizable electrode/region 160 interface is greater than the resistance at any other point along region 160, particularly, the interface between region 160 and the indifferent electrode.

One way to achieve relatively low resistance at the indifferent electrode is to form the electrode of relatively inert, non-oxidizing material such as platinum. Use of such material reduces formation of oxides at the interface between ion conductor 140 and the indifferent electrode as well as the formation of compounds or mixtures of the electrode material and ion conductor 140 material, which typically have a higher resistance than ion conductor 140 or the electrode material.

Relatively low resistance at the indifferent electrode may also be obtained by forming a barrier layer between the oxidizable electrode (anode during a write operation) and the ion conductor, wherein the barrier layer is formed of material having a relatively high resistance. Exemplary high resistance materials are discussed in more detail below.

Reliable growth and dissolution of region 160 can also be facilitated by providing a roughened indifferent electrode surface (e.g., a root mean square roughness of greater than about 1 nm) at the electrode/ion conductor interface. The roughened surface may be formed by manipulating film deposition parameters and/or by etching a portion of one of the electrode or ion conductor surfaces. During a write operation, relatively high electrical fields form about the spikes or peaks of the roughened surface, and thus regions 160 are more likely to form about the spikes or peaks. As a result, more reliable and uniform changes in electrical properties for an applied voltage across electrodes 120 and 130 may be obtained by providing a roughed interface between the indifferent electrode (cathode during a write operation) and ion conductor 140.

Oxidizable electrode material may have a tendency to thermally dissolve or diffuse into ion conductor 140, particularly during fabrication and/or operation of structure 100. The thermal diffusion is undesired because it may reduce the resistance of structure 100 and thus reduce the change of an electrical property during use of structure 100.

To reduce undesired diffusion of oxidizable electrode material into ion conductor 140 and in accordance with another embodiment of the invention, the oxidizable electrode includes a metal intercalated in a transition metal sulfide or selenide material such as $A_x(MB_2)_{1-x}$, where A is Ag or Cu, B is S or Se, M is a transition metal such as Ta, V, and Ti, and x ranges from about 0.1 to about 0.7. The intercalated material mitigates undesired thermal diffusion of the metal (Ag or Cu) into the ion conductor material, while allowing the metal to participate in region 160 growth upon application of a sufficient voltage across electrodes 120 and 130. For example, when silver is intercalated into a $TaS_2$ film, the $TaS_2$ film can include up to about 67 atomic percent silver. The $A_x(MB_2)_{1-x}$ material is preferably amorphous to prevent undesired diffusion of the metal though the material. The amorphous material may be formed by, for example, physical vapor deposition of a target material comprising $A_x(MB_2)_{1-x}$.

α-AgI is another suitable material for the oxidizable electrode. Similar to the $A_x(MB_2)_{1-x}$ material discussed above, α-AgI can serve as a source of Ag during operation of structure 100—e.g., upon application of a sufficient bias, but the silver in the AgI material does not readily thermally diffuse into ion conductor 140. AgI has a relatively low activation energy for conduction of electricity and does not require doping to achieve relatively high conductivity. When the oxidizable electrode is formed of AgI, depletion of silver in the AgI layer may arise during operation of structure 100, unless excess silver is

provided to the electrode. One way to provide the excess silver is to form a silver layer adjacent the AgI layer. When interposed between a layer of silver and ion conductor 140, the AgI layer reduces thermal diffusion of Ag into ion conductor 140, but does not significantly affect conduction of Ag during operation of structure 100. In addition, use of AgI increases the operational efficiency of structure 100 because the AgI mitigates non-Faradaic conduction (conduction of electrons that do not participate in the electrochemical reaction).

In accordance with one embodiment of the invention, at least one electrode 120 and 130 is formed of material suitable for use as an interconnect metal. For example, electrode 130 may form part of an interconnect structure within a semiconductor integrated circuit. In accordance with one aspect of this embodiment, electrode 130 is formed of a material that is substantially insoluble in material comprising ion conductor 140. Exemplary materials suitable for both interconnect and electrode 130 material include metals and compounds such as tungsten, nickel, molybdenum, platinum, metal silicides, and the like.

As noted above, programmable structures of the present invention may include one or more barrier or buffer layers 155, 255 interposed between at least a portion of ion conductor 140 and one of the electrodes 120, 130. Layers 155, 255 may include ion conductors such as $Ag_xO$, $Ag_xS$, $Ag_xSe$, $Ag_xTe$, where $x \geq 2$, $Ag_yI$, where $x \geq 1$, $CuI_2$, CuO, CuS, CuSe, CuTe, $GeO_2$, $Ge_zS_{1-z}$, $Ge_zSe_{1-z}$, $Ge_zTe_{1-z}$, $As_zS_{1-z}$, $As_zSe_{1-z}$, $As_zTe_{1-z}$, where z is greater than or equal to about 0.1, $SiO_x$, and combinations of these materials) interposed between ion conductor 140 and a metal layer such as silver.

Other materials suitable for buffer layers 155 and/or 255 include $GeO_2$. Amorphous $GeO_2$ is relatively porous an will "soak up" silver during operation of device 100, but will retard the thermal diffusion of silver to ion conductor 140, compared to structures or devices that do not include a buffer layer. When ion conductor 140 includes germanium, $GeO_2$ may be formed by exposing ion conductor 140 to an oxidizing environment at a temperature of about 300 °C to about 800 °C or by exposing ion conductor 140 to an oxidizing environment in the presence of radiation having an energy greater than the band gap of the ion conductor material. The $GeO_2$ may also be deposited using physical vapor deposition (from a $GeO_2$ target) or chemical vapor deposition (from $GeH_4$ and an $O_2$).

Buffer layers can also be used to increase the off resistance and "write voltage" by placing a high-resistance buffer layer (e.g., $GeO_2$, $SiO_x$, air, a vacuum, or the like) between ion conductor 140 and the indifferent electrode. In this case, the high-resistance buffer

material allows metal such as silver to diffuse though or plate across the buffer and take part in the electrochemical reaction.

When the barrier layer between the indifferent electrode and the ion conductor includes a high resistance material, the barrier may include ions that contribute to electrodeposit growth or the barrier may be devoid of ions. In either case, the barrier must be able to transmit electrons, by conduction or tunneling, such that the redox reaction occurs, allowing for region 160 growth.

In some cases, an electrodeposit may form within the high-resistance barrier layer. Exemplary high-resistance barrier layers that support electrodeposit growth include gas-filled or vacuum gap regions, porous oxide films, of other high-resistance glassy materials, and semiconductor material as long as the barrier is thin enough to allow electron tunneling from the cathode to the ion conductor at reasonable voltages (e.g., less than or equal to about 1 volt), can support electron transport, and can allow ions to be reduced within the barrier material volume.

Layers 155 and/or 255 may also include a material that restricts migration of ions between conductor 140 and the electrodes. In accordance with exemplary embodiments of the invention, a barrier layer includes conducting material such as titanium nitride, titanium tungsten, a combination thereof, or the like. The barrier may be electrically indifferent, *i.e.*, it allows conduction of electrons through structure 100 or 200, but it does not itself contribute ions to conduction through structure 200. An electrically indifferent barrier may reduce undesired electrodeposit growth during operation of the programmable device, and thus may facilitate an "erase" or dissolution of region 160 when a bias is applied which is opposite to that used to grow region 160. In addition, use of a conducting barrier allows for the "indifferent" electrode to be formed of oxidizable material because the barrier prevents diffusion of the electrode material to the ion conductor.

Ion conductor 140 is formed of material that conducts ions upon application of a sufficient voltage. Suitable materials for ion conductor 140 include glasses and semiconductor materials. In one exemplary embodiment of the invention, ion conductor 140 is formed of chalcogenide material.

Ion conductor 140 may also suitably include dissolved conductive material. For example, ion conductor 140 may comprise a solid solution that includes dissolved metals and/or metal ions. In accordance with one exemplary embodiment of the invention, conductor 140 includes metal and/or metal ions dissolved in chalcogenide glass. An

exemplary chalcogenide glass with dissolved metal in accordance with the present invention includes a solid solution of $As_xS_{1-x}$-Ag, $As_xSe_{1-x}$-Ag, $As_xTe_{1-x}$-Ag, $Ge_xSe_{1-x}$-Ag, $Ge_xS_{1-x}$-Ag, $Ge_xTe_{1-x}$-Ag, $As_xS_{1-x}$-Cu, $As_xSe_{1-x}$-Cu, $As_xTe_{1-x}$-Cu, $Ge_xSe_{1-x}$-Cu, $Ge_xS_{1-x}$–Cu, and $Ge_xTe_{1-x}$-Cu where x ranges from about 0.1 to about 0.5, other chalcogenide materials including silver, copper, combinations of these materials, and the like. In addition, conductor 140 may include network modifiers that affect mobility of ions through conductor 140. For example, materials such as metals (*e.g.*, silver), halogens, halides, or hydrogen may be added to conductor 140 to enhance ion mobility and thus increase erase/write speeds of the structure. Furthermore, as discussed in more detail below, ion conductor 140 may include a plurality of regions having different resistance values--for example, ion conductor 140 may include a first region proximate the oxidizable electrode having a relatively low resistance and a second region proximate the indifferent electrode having a relatively high resistance.

To increase the thermal stability of ion conductor, doped oxides and/or oxide-doped chalcogenides are used as ion conductor 140. Exemplary oxide dopants for chalcogenide materials include oxygen, $GeO_2$, $As_2O_3$, $Ag_2O$, $Cu_{(1,2)}O$, and $SiO_2$ and exemplary oxides suitable for doping include silver or copper doped $GeO_2$, $As_2O_3$, $Ag_2O$, $Cu_{(1,2)}O$, and $SiO_x$. In the case of doped oxides, ion conductor 140 is preferably less than about 10 nm thick.

Ion conductor 140 may also include a filler material, which fills interstices or voids. Suitable filler materials include non-oxidizable and non-silver based materials such as a non-conducting, immiscible silicon oxide and/or silicon nitride, having a cross-sectional dimension of less than about 1 nm, which do not contribute to the growth of region 160. In this case, the filler material is present in the ion conductor at a volume percent of up to about 5 percent to reduce a likelihood that a region 160 will spontaneously dissolve into the supporting ternary material as the device is exposed to elevated temperature, which leads to more stable device operation without compromising the performance of the device. Ion conductor 140 may also include filler material to reduce an effective cross-sectional area of the ion conductor. In this case, the concentration of the filler material, which may be the same filler material described above but having a cross-sectional dimension up to about 50 nm, is present in the ion conductor material at a concentration of up to about 50 percent by volume.

In accordance with one exemplary embodiment of the invention, ion conductor 140 includes a germanium-selenide glass with silver diffused in the glass. Germanium selenide materials are typically formed from selenium and $Ge(Se)_{4/2}$ tetrahedra that may combine in a

variety of ways. In a Se-rich region, Ge is 4-fold coordinated and Se is 2-fold coordinated, which means that a glass composition near $Ge_{0.20}Se_{0.80}$ will have a mean coordination number of about 2.4. Glass with this coordination number is considered by constraint counting theory to be optimally constrained and hence very stable with respect to devitrification. The network in such a glass is known to self-organize and become stress-free, making it easy for any additive, e.g., silver, to finely disperse and form a mixed-glass solid solution. Accordingly, in accordance with one embodiment of the invention, ion conductor 140 includes a glass having a composition of $Ge_{0.17}Se_{0.83}$ to $Ge_{0.25}Se_{0.75}$.

When conductive material such as metal is added to an ion conductor material, phase-separated regions of the metal-doped ion conductor may form. In this case, a macroscopic view of the doped ion conductor may appear glassy even though small, phases-separated regions are formed.

Figures 3-5 illustrate portions of programmable structures, which include phase-separated ion conductor material, in accordance with various embodiments of the present invention. Figure 3 illustrates a phase-separated ion conductor region 302, including a high-resistance portion 304 and low-resistance portions 306. By way of particular example, when ion conductor 302 includes silver doped $Ge_xSe_{1-x}$, where x preferably ranges from about 0.17 to about 0.3 and more preferably has a value of about 0.17 to about 0.25, ion conductor separates into a first phase 304 of Ge-Se (e.g., $Ge_2Se_3$) and a second phase 306 of $Ag_2Se$, which is much more conductive that Ge-Se portion 304. Phase-separated ion conductor 302 has an overall resistivity of about 100 ohm-cm and is stable at room temperature.

It is thought that phase-separated ion conductors facilitate large off resistance and high switching speed of programmable devices such as device 100. The reason for this is that the metal ions from the soluble electrode will migrate within region 304 to bridge low-resistance regions 306. Reduction of metal ions preferentially occurs in high-resistance regions 304 because the local field is highest in this area of ion conductor 302. This process is relatively fast because a typical gap between low-resistance portions is on the order of about 1 nm or less.

Other exemplary materials suitable for phase-separated ion-conductor material include silver and/or copper-doped germanium chalcogenides (e.g., sulfides and tellurides) and mixtures of these compounds, silver and/or copper-doped arsenic chalcogenides (e.g., selenides, sulfides, and tellurides) and mixtures of these compounds. Other exemplary phase-separate ion conductors include $Ag_2Se$ dispersed within AgI or within an ion

conductive polymer such as poly(ethylene oxide) and additional exemplary low-resistance material suitable for portion 304 include $SiO_x$, $GeO_2$, and $Ag_2O$. It should be noted, however, that any ion conductor material that includes a low-resistance phase dispersed within a low-resistance phase will function in accordance with the present invention as described herein.

Figure 4 illustrates a structure 400, including a phase-separated ion conductor 402. Ion conductor 402 includes high-resistance portions 404 and low-resistance portions 406. Portions 404 and 406 may be formed of corresponding high-resistance and low-resistance material described above in connection with portions 304 and 306. Structure 400 may be formed by sequentially depositing high-resitivity material and low-resistance material. Although illustrated with only two high-resistance portions and two low-resistance portions, structures in accordance with the present invention may include any desired number of low and high-resistivity portions.

Similar to the operation of structure 300, the operation speed of structure 400 is primarily limited by the change of resistance of high-resistance portions 404. Accordingly, operational speed of structures 400 can be manipulated by altering a thickness of layer(s) 404.

Figure 5 illustrates another structure 500, which includes phase separated ion conductor material 502. Structure 500 is similar to structures 300 and 400, except that structure 500 includes particles 508, including a high-resistance portion 504 and a low-resistance portion 506, which may be formed of low and high-resistance materials described herein.

Referring again to Figures 1 and 2, in accordance with one exemplary embodiment of the invention, at least a portion of structure 100 is formed within a via of an insulating material 150. Forming a portion of structure 100 within a via of an insulating material 150 may be desirable because, among other reasons, such formation allows relatively small structures, *e.g.*, on the order of 10 nanometers, to be formed. In addition, insulating material 150 facilitates isolating various structures 100 from other electrical components.

Insulating material 150 suitably includes material that prevents undesired diffusion of electrons and/or ions from structure 100. In accordance with one embodiment of the invention, material 150 includes silicon nitride, silicon oxynitride, polymeric materials such as polyimide or parylene, or any combination thereof.

A contact 165 may suitably be electrically coupled to one or more electrodes 120, 130 to facilitate forming electrical contact to the respective electrode. Contact 165 may be formed of any conductive material and is preferably formed of a metal, alloy, or composition including aluminum, tungsten, or copper.

In accordance with one embodiment of the invention, structure 100 is formed by forming electrode 130 on substrate 110. Electrode 130 may be formed using any suitable method such as, for example, depositing a layer of electrode 130 material, patterning the electrode material, and etching the material to form electrode 130. Insulating layer 150 may be formed by depositing insulating material onto electrode 130 and substrate 110 and forming vias in the insulating material using appropriate patterning and etching processes. Ion conductor 140 and electrode 120 may then be formed within insulating layer 150 by depositing ion conductor 140 material and electrode 120 material within the via. Such ion conductor and electrode material deposition may be selective – *i.e.*, the material is substantially deposited only within the via, or the deposition processes may be relatively non-selective. If one or more non-selective deposition methods are used, any excess material remaining on a surface of insulating layer 150 may be removed using, for example, chemical mechanical polishing and/or etching techniques. Barrier layers 155 and/or 255 may similarly be formed using any suitable deposition and/or etch processes.

A solid solution suitable for use as ion conductor 140 may be formed in a variety of ways. For example, the solid solution may be formed by depositing a layer of conductive material such as metal over a chalcogenide glass and exposing the metal and glass to thermal and/or photo dissolution processing. In accordance with one exemplary embodiment of the invention, a solid solution of $As_2S_3$-Ag is formed by depositing $As_2S_3$ onto a substrate, depositing a thin film of Ag onto the $As_2S_3$,, and exposing the films to light having energy greater than the optical gap of the $As_2S_3$,--*e.g.*, light having a wavelength of less than about 500 nanometers. If desired, network modifiers may be added to conductor 140 during deposition of conductor 140 (*e.g.*, the modifier is in the deposited material or present during conductor 140 material deposition) or after conductor 140 material is deposited (*e.g.*, by exposing conductor 140 to an atmosphere including the network modifier).

In accordance with another embodiment of the invention, a solid solution may be formed by depositing one of the constituents from a source onto a substrate or another material layer and reacting the first constituent with a second constituent. For example, germanium (preferably amorphous) may be deposited onto a portion of a substrate and the

germanium may be reacted with $H_2Se$ to form a Ge-Se glass. Similarly, As can be deposited and reacted with the $H_2Se$ gas, or arsenic or germanium can be deposited and reacted with $H_2S$ gas. Silver or other metal can then be added to the glass as described above.

When used, oxides may be added to the ion conductor material by adding an oxide to a melt used to form a chalcogenide ion conductor source. For example, $GeO_2$, $As_2O_3$, $Ag_2O$, $Cu_{(1,2)}O$, and $SiO_2$, can be added to $Ge_xS_{1-x}$, $As_xS_{1-x}$, $Ge_xSe_{1-x}$, $As_xSe_{1-x}$, $Ge_xTe_{1-x}$, $As_xTe_{1-x}$ to form an oxide-chalcogenide glass including up to several tens of atomic percent oxygen. The ternary or quaternary glass can then be used to deposit a film of similar composition on the device substrate by physical vapor deposition or similar technique. Alternatively, the oxygen-containing film may be formed in-situ using reactive deposition techniques in which the chalcogenide material is deposited in a reactive oxygen ambient to form an ion conductor including up to several tens of atomic percent of bound oxygen. Conductive material such as silver or copper can be incorporated into the source glass melt or introduced into the deposited film by thermal or photo-dissolution as discussed above.

Similarly, metal doped oxides may be deposited from a synthesized source which contains all the necessary elements in the correct proportions (e.g., $Ag_xO$ ($x>2$), $Cu_xO$ ($x>2$), Ag/Cu-$GeO_2$, Ag/Cu-$As_2O_3$, or Ag/Cu-$SiO_2$) or the silver or copper may be introduced into the binary oxide film ($Ag_2O$, $Cu_{(1,2)}O$, $GeO_2$, $As_2O_3$, or $SiO_2$) by thermal- or photo-dissolution from a thin surface layer of the metal. Alternatively, a base layer of Ag, Cu, Ge, As, or Si may be deposited first and then reacted with oxygen to form the appropriate oxide and then diffused with Ag or Cu as discussed above. The oxygen reaction could be purely thermal or plasma-assisted, the latter producing a more porous oxide.

One of the electrodes may be formed during ion conductor 140 doping by depositing sufficient metal onto an ion conductor material and applying sufficient electrical or thermal energy to the layers such that a portion of the metal is dissolved within the ion conductor material and a portion of the metal remains on a surface of the ion conductor to form an electrode (*e.g.*, electrode 120). Regions of differing conductivity within ion conductor 140 can be formed using this technique by applying a sufficient amount of energy to the structure such that a first portion of the ion conductor proximate the soluble electrode contains a greater amount of conductive material than a second portion of the ion conductor proximate the indifferent electrode. This process is self limiting if ion starting ion conductor layer is thick enough so that a portion of the film becomes saturated and a portion of the film is unsaturated.

In accordance with alternative embodiments of the invention, solid solutions containing dissolved metals may be directly deposited onto substrate 110 and the electrode then formed overlying the ion conductor. For example, a source including both chalcogenide glass and conductive material can be used to form ion conductor 140 using physical vapor deposition or similar techniques.

An amount of conductive material such as metal dissolved in an ion conducting material such as chalcogenide may depend on several factors such as an amount of metal available for dissolution and an amount of energy applied during the dissolution process. However, when a sufficient amount of metal and energy are available for dissolution in chalcogenide material using photodissolution, the dissolution process is thought to be self limiting, substantially halting when the metal cations have been reduced to their lowest oxidation state. In the case of $As_2S_3$-Ag, this occurs at $Ag_4As_2S_3 = 2Ag_2S + As_2S$, having a silver concentration of about 44 atomic percent. If, on the other hand, the metal is dissolved in the chalcogenide material using thermal dissolution, a higher atomic percentage of metal in the solid solution may be obtained, provided a sufficient amount of metal is available for dissolution.

In accordance with a further embodiment of the invention, the solid solution is formed by photodissolution to form a macrohomogeneous ternary compound and additional metal is added to the solution using thermal diffusion (e.g., in an inert environment at a temperature of about 85 °C to about 150 °C) to form a solid solution containing, for example, about 30 to about 50, and preferably about 34 atomic percent silver. Ion conductors having a metal concentration above the photodissolution solubility level facilitates formation of regions 160 that are thermally stable at operating temperatures (typically about 85 °C to about 150 °C) of devices 100 and 200. Alternatively, the solid solution may be formed by thermally dissolving the metal into the ion conductor at the temperature noted above; however, solid solutions formed exclusively from photodissolution are thought to be less homogeneous than films having similar metal concentrations formed using photodissolution and thermal dissolution.

Information may be stored using programmable structures of the present invention by manipulating one or more electrical properties of the structures. For example, a resistance of a structure may be changed from a "0" or off state to a "1" or on state during a suitable write operation. Similarly, the device may be changed from a "1" state to a "0" state during an erase operation. In addition, as discussed in more detail below, the structure may have

multiple programmable states such that multiple bits of information are stored in a single structure.

WRITE OPERATION

Figure 6 illustrates current-voltage characteristics of a programmable structure (e.g. structure 200) in accordance with the present invention. In the illustrated embodiment, via diameter, D, is about 4 microns, conductor 140 is about 35 nanometers thick and formed of $Ge_3Se_7$-Ag (near $Ag_8Ge_3Se_7$), electrode 130 is indifferent and formed of nickel, electrode 120 is formed of silver, and barrier 255 is a native nickel oxide. As illustrated in Figure 6, current through structure 200 in an off state (curve 610) begins to rise upon application of a bias of over about one volt; however, once a write step has been performed (*i.e.*, an electrodeposit has formed), the resistance through conductor 140 drops significantly (*i.e.*, to about 200 ohms), illustrated by curve 620 in Figure 6. As noted above, when electrode 130 is coupled to a more negative end of a voltage supply, compared to electrode 120, a conductive region begins to form near electrode 130 and grow toward electrode 120. An effective threshold voltage (*i.e.*, voltage required to cause growth of the conductive region and to break through barrier 255, thereby coupling electrodes 120, 130 together) is relatively high because of barrier 255. In particular, a voltage $V \geq V_T$ must be applied to structure 200 sufficient to cause electrons to tunnel through barrier 255 (when barrier 255 comprises an insulating layer) to form the conductive region and to overcome the barrier (e.g., by tunneling through or leakage) and conduct through conductor 140 and at least a portion of barrier 255.

In accordance with alternate embodiments of the invention, where no insolating barrier layer is present, an initial "write" threshold voltage is relatively low because no insulative barrier is formed between, for example, ion conductor 140 and either of the electrodes 120, 130.

As noted above, the relative volatility of the memory structures of the present invention may be altered by applying different amounts of energy to the structures during a write process. For example, a relatively high current pulse of a few hundred microamperes for a period of about several hundred nanoseconds may be applied to the structures illustrated in Figures 1 and 2 to form a relatively nonvolatile memory cell. Alternatively, the same current may be supplied to the same or similar memory structure for a shorter amount of time, e.g., several nanoseconds to form a relatively volatile memory structure. In either

case, the memory of the present invention can be programmed at relatively high speeds and even the "volatile" memory is relatively nonvolatile compared to traditional DRAM. For example, the volatile memory may operate at speed comparable to DRAM and only require refreshing every several hours.

5

READ OPERATION

A state of a memory cell (*e.g.*, 1 or 0) may be read, without significantly disturbing the state, by, for example, applying a forward or reverse bias of magnitude less than a voltage threshold (about 1.4 V for a structure illustrated in Figure 6) for electrodeposition or 10 by using a current limit which is less than or equal to the minimum programming current (the current which will produce the highest of the on resistance values). A current limited (to about 1 milliamp) read operation is illustrated in Figure 6. In this case, the voltage is swept from 0 to about 2 V and the current rises up to the set limit (from 0 to 0.2 V), indicating a low resistance (ohmic/linear current-voltage) "on" state. Another way of 15 performing a non-disturb read operation is to apply a pulse, with a relatively short duration, which may have a voltage higher than the electrochemical deposition threshold voltage such that no appreciable Faradaic current flows, *i.e.*, nearly all the current goes to polarizing/charging the device and not into the electrodeposition process.

In accordance with various embodiments of the invention, circuits including the 20 programmable structures include temperature compensation devices to mitigate effects of temperature variation on the performance of the programmable device. One exemplary temperature compensation circuit includes a programmable structure having a known erased state. In this case, during a read operation, a progressively increasing voltage is applied to a programmable structure having an unknown state as well as to the structure having the 25 known erased state. If the unknown structure has been written to, it will switch on before the known erased device and if the unknown structure is in an erased state, the two devices will switch on at approximately the same time. Alternatively, a temperature compensation circuit can be used to produce a comparison voltage or current to be compared to a voltage or current produced by a programmable structure of an unknown state during a read process.

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ERASE OPERATION

A programmable structure (*e.g.*, structure 200) may suitably be erased by reversing a bias applied during a write operation, wherein a magnitude of the applied bias is equal to or

greater than the threshold voltage for electrodeposition in the reverse direction. In accordance with an exemplary embodiment of the invention, a sufficient erase voltage ($V \geq V_T$) is applied to structure 200 for a period of time, which depends on energy supplied during the write operation, but is typically less than about 1 millisecond to return structure 200 to its "off" state having a resistance well in excess of a million ohms. In cases where the programmable structure does not include a barrier between conductor 140 and electrode 120, a threshold voltage for erasing the structure is much lower than a threshold voltage for writing the structure because, unlike the write operation, the erase operation does not require electron tunneling through a barrier or barrier breakdown.

CONTROL OF OPERATIONAL PARAMETERS

The concentration of conductive material in the ion conductor can be controlled by applying a bias across the programmable device. For example, metal such as silver may be taken out of solution by applying a negative voltage in excess of the reduction potential of the conductive material. Conversely, conductive material may be added to the ion conductor (from one of the electrodes) by applying a bias in excess of the oxidation potential of the material. Thus, for example, if the conductive material concentration is above that desired for a particular device application, the concentration can be reduced by reverse biasing the device to reduce the concentration of the conductive material. Similarly, metal may be added to the solution from the oxidizable electrode by applying a sufficient forward bias. Additionally, it is possible to remove excess metal build up at the indifferent electrode by applying a reverse bias for an extended time or an extended bias over that required to erase the device under normal operating conditions. Control of the conductive material may be accomplished automatically using a suitable microprocessor.

With particular reference to Figures 3-5, a partial write or a partial erase caused by a forward or reverse programming pulse of insufficient duration and/or current to introduce enough silver to significantly reduce the resistance of the high-resistance regions will cause additional silver to migrate from the soluble electrode the high-resistance portions. The conductivity and activation energy in these zones are altered by this excess silver even though the device will appear to be in a high resistance state. The change in activation energy results in higher ion mobility and hence this partial preprogramming results in much faster switching than in a device which had been fully written or erased, which in turn allows appropriately scaled devices to operate at SRAM speeds (in the nanosecond or less range).

In addition, in a written device that has "faded" due to thermal diffusion of the electrodeposited material away from the low resistance pathway, the local excess silver will still promote a lower activation energy but in this case, there is also sufficient silver present that the voltage required to reform the conducting link will be lower than in the case of a normal write. The "reclosure" voltage will be several tens of mV lower than the redox potential of the system since the silver required to close the link is already in the material and does not have to be released from the oxidizable electrode. This means that a simple "read" operation involving a short pulse below the redox potential will be sufficient to regenerate a faded on-state in the device but will be insufficient to disturb a device that has been fully erased (and hence does not have the excess silver). This will allow faded lightly written (low programming current) states to be automatically regenerated by the read operation, thereby extending the effective retention of the devices.

This technique may also be used to form one of the electrodes from material within the ion conductor material. For example, silver from the ion conductor may be plated out to form the oxidizable electrode. This allows the oxidizable electrode to be formed after the device is fully formed and thus mitigates problems associated with conductive material diffusing from the oxidizable electrode during manufacturing of the device.

The threshold voltage of programmable devices may be manipulated in accordance with various embodiments of the present invention. Manipulation of the threshold voltage allows configuration of the programmable devices for desired read and write voltages. In general, as noted above, the threshold voltage depends on, among other things, an amount of conductive material present in the ion conductor and/or any barrier.

One way to manipulate the electrodeposition threshold voltage is to manipulate the conductive material dispersed within the ion conductor material. Another technique for manipulating the threshold voltage is to alter an amount of oxidizable material at or near the indifferent electrode. In this case, the oxidizable metal at the cathode can be altered by first forming an electrodeposit at or near the indifferent electrode and then applying a reverse bias sufficient to dissolve a portion of the electrodeposit. The threshold voltage generally goes down as the amount of oxidizable metal at the cathode goes up. For example, in the case where the ion conductor is $Ge_{0.3}Se_{0.7}$ and the soluble electrode is silver, the threshold voltage for electrodeposit formation is about 310 ±10 mV for no predeposited silver to about 90 ± 10 mV for a silver saturated electrode. Alternatively, a write process may be used to form a desired electrodeposit at or near the cathode. This electrochemical control of the threshold

voltage can be used to heal or regenerate an electrodeposit that has been thermally or electrochemically damaged or redistributed. As an example of how this would work, consider the following:

1. An electrodeposit can be formed in or on the electrolyte using a write voltage that is determined by the Ag concentration near the cathode, e.g., 0.32 V for a silver depleted cathode region.

2. A read voltage below the write voltage may be used to determine the state of the device without disturbing an off device.

3. The electrodeposit is subsequently "damaged" by thermal diffusion (e.g., excessive external device heating) so that the electrodeposit is no longer continuous or localized.

4. The Ag concentration near the cathode will still be higher than in the case of an unwritten or completely erased device as the silver cannot diffuse against the diffusion gradient.

5. The increased cathodic silver results in a reduction of the re-write voltage, e.g., below the read voltage which is chosen not to disturb an off state but to be high enough to "regenerate" most failed electrodeposits.

Therefore, a read operation can be used to automatically re-electrodeposit the silver and regenerate the data state stored in the device via the electrodeposited material. This will ensure that the programmable structures effectively retain data for extended periods of time.

Another technique for manipulating threshold voltage is by forming a layer of material between the indifferent electrode and the ion conductor layer, wherein the layer of material is capable of conducting ions and forming an electrodeposit and has a lower concentration of oxidizable material than the ion conductor. Exemplary materials suitable for this layer include undoped or lightly doped chalcogenide materials such as Ge-S or Ge-Se and a variety of other undoped or lightly doped ion conductor materials that have a low solubility level for the oxidizable material. The material layer between the indifferent electrode and the ion conductor reduces oxidizable material build up neat the indifferent electrode during processing and operation of the programmable structure.

An example of a write operation on a device which includes a silver saturated sulfur-rich Ge-S starting glass and a layer of relatively low silver content, less than 10 nm thick, between the indifferent electrode and the saturated ion conductor is illustrated in Figure 7 (current vs. voltage for a 1 μA programming current) and Figure 8 (resistance vs. voltage for

a 1 μA programming current). In the illustrated case, the write voltage lies around 320 mV. Note that this layer could be deposited separately from the Ag-rich electrolyte or can be formed, as described above, by stopping the photodiffusion before the oxidazable metal penetrates the entire film thickness.

To mitigate undesired diffusion of an electrodeposit formed during a write process, it may be desired to saturate the ion conductor with conductive material during a write process, such that the resistance of the structure does not substantially change due to diffusion of conductive material. In the case where the ion conductor comprises germanium selenide doped with silver and the electrodeposit is formed from silver, the approximate minimum "saturation" programming current to maintain electrodeposition until the electrolyte has a uniform silver concentration and corresponding resistance as a function of electrolyte area is given below for a 10 nm thick silver-doped germanium selenide solid electrolyte.

| Area ($nm/nm^2$) | Saturation current (μA) | Resistance (kΩ) |
|---|---|---|
| 1 | 0.3 | 1,000 |
| 10 | 3 | 100 |
| 100 | 30 | 10 |
| 1000 | 300 | 1 |
| 10,000 | 3,000 | 0.1 |

Figures 9-10 illustrate additional structures, which are configured to mitigate any unwanted diffusion of conductive material within an ion conductor, in accordance with further exemplary embodiments of the present invention. In general, the structures illustrated in Figures 9-10 include a relatively narrow ion conductor (compared to the height of the ion conductor) surrounded by a material which is less ion conductive than the ion conductor.

Structure 900 includes a first electrode 902, an insulating layer 904, a diffusion barrier 906, an ion conductor 908 and a second electrode 910. Electrodes 902 and 910, insulating layer 904, and ion conductor 908 may be formed of the corresponding materials and using the same techniques described above in connection with Figures 1 and 2. The barriers may be configured such that only one "column" of ion conductor material spans between the electrodes or the structures may include a plurality of ion conductor columns that span between the electrodes. In the latter case, the electrodeposition may only occur in

one of the columns if the current is appropriately limited. In either case, because the column diameter is relatively small (e.g., less than about 50 nm) the current required to saturate the region is also relatively small (e.g., about 30 μA).

Diffusion barrier 906 can be formed by conformally depositing a barrier material 1002 such as silicon nitride or any of the barrier materials discussed above in connection with layer 155 and 255 and illustrated in Figure 10 and removing a portion of the barrier material (e.g., using an anisotropic etch) to form barrier 906 illustrated in Figure 9. Ion conductor 908 can then be formed using deposition and etch or damascene techniques.

Another technique for forming diffusion barriers is illustrated in Figures 11 and 12. In this case, porous barrier material 1102 is formed on a surface of a substrate 1104 and ion conductor material is formed in the porous regions of barrier material 1102. Alternatively, porous material 1102 can be used as an etch mask to etch ion conductor material (using an anisotropic etch) to form columns of ion conductor material. Spaces between to columns are then filled with appropriate barrier maters such as silicon nitride. Electrodes may be formed about one or more columns of ion conductor material as described herein to form programmable devices of the present invention.

Figure 13 illustrates yet another structure 1300 suitable for forming diffusion-resistant programmable structures. Structure 1300 includes a first electrode 1302, a second electrode 1304, an ion conductor 1306, and a material layer 1308 that favors electrodeposit growth substantially in only one direction. Electrodes 1302 and 1304 and ion conductor 1306 may be formed of any of the corresponding electrodes and ion conductors described herein. Suitable exemplary materials for material layer 1308 include thin (e.g. a few nm) amorphous films of oxides and nitrides (e.g., $SiO_2$, $GeO_2$, $Si_3N_4$) and semiconductors (Si, Ge) and polycrystalline films of oxides, nitrides, and semiconductors. In accordance with one aspect of this embodiment of the invention, layer 1308 is formed between ion conductor 1306 and the indifferent electrode.

As noted above, in accordance with yet another embodiment of the invention, multiple bits of data may be stored within a single programmable structure by controlling a size of region 160 which is formed during a write process. A size of region 160 that forms during a write process depends on a number of coulombs or charge supplied to the structure during the write process, and may be controlled by using a current limit power source. In this case, a resistance of a programmable structure is governed by Equation 1, where $R_{on}$ is

the "on" state resistance, $V_T$ is the threshold voltage for electrodeposition , and $I_{LIM}$ is the maximum current allowed to flow during the write operation.

$$R_{on} = \frac{V_T}{I_{LIM}}$$

Equation 1

In practice, the limitation to the amount of information stored in each cell will depend on how stable each of the resistance states is with time. For example, if a structure with a programmed resistance range of about 3.5 kΩ and a resistance drift over a specified time for each state is about ±250 Ω, about 7 equally sized bands of resistance (7 states) could be formed, allowing 3 bits of data to be stored within a single structure. In the limit, for near zero drift in resistance in a specified time limit, information could be stored as a continuum of states, *i.e.*, in analog form.

A portion of an integrated circuit 1402, including a programmable structure 1400, configured to provide additional isolation from electronic components is illustrated in Figure 14. Structure 1400 includes electrodes 1420 and 1430, an ion conductor 1440, a contact 1460, and an amorphous silicon diode 1470, such as a Schottky or p-n junction diode, formed between contact 1460 and electrode 1420. Rows and columns of programmable structures 1400 may be fabricated into a high density configuration to provide extremely large storage densities suitable for memory circuits. In general, the maximum storage density of memory devices is limited by the size and complexity of the column and row decoder circuitry. However, a programmable structure storage stack can be suitably fabricated overlying an integrated circuit with the entire semiconductor chip area dedicated to row/column decode, sense amplifiers, and data management circuitry (not shown) since structure 1400 need not use any substrate real estate. In this manner, storage densities of many gigabits per square centimeter can be attained using programmable structures of the present invention. Utilized in this manner, the programmable structure is essentially an additive technology that adds capability and functionality to existing semiconductor integrated circuit technology.

Figure 15 schematically illustrates a portion of a memory device including structure 1400 having an isolating p-n junction 1470 at an intersection of a bit line 1510 and a word line 1520 of a memory circuit. Figure 16 illustrates an alternative isolation scheme employing a transistor 1610 interposed between an electrode and a contact of a programmable structure located at an intersection of a bit line 1610 and a word line 1620 of a memory device.

Figures 17-20 illustrate programmable devices in accordance with another embodiment of the invention. The devices illustrated in Figures 17-20 have an electrode (e.g., the cathode during a write process) with a smaller cross sectional area in contact with the ion conductor compared to the devices illustrated in Figures 1 and 2. The smaller electrode interface area is thought to increase the efficiency and endurance of the device because an increased percentage of ions in the solid solution are able to take part in regions 160 formation process. Thus any cathode plating from ions that do not participate in region 160 formation process is reduced.

Figures 17 and 18 illustrate a cross sectional and a top cut-away view of a programmable device 1700 including an indifferent electrode 1710, an oxidizable electrode 1720, and an ion conductor 1730 formed overlying an insulating layer 1740 such as silicon oxide, silicon nitride, or the like.

Structure 1700 is formed by depositing an indifferent electrode material layer and an insulating layer 1750 overlying insulating layer 1740. A via is then formed through layer 1750 and electrode material layer 1710, using an anisotropic etch process (e.g., reactive ion etching or ion milling) such that the via extends to and/or through a portion of layer 1740. The via is then filled with ion conductor material and is suitably doped to form a solid solution as described herein. Any excess ion conductor material is removed from the surface of layer 1750 and electrode 1730 is formed using, for example, a deposition and etch process. In this case, the indifferent electrode area in contact with ion conductor 1730 is the surface area of electrode 1710 about the perimeter of conductor 1730, rather than the area underlying the ion conductor, as illustrated in Figures 1 and 2.

Figures 19 and 20 illustrate a programmable device 1900 having an indifferent electrode 1910, an oxidizable electrode 1920, an ion conductor 1930 and insulating layers 1940 and 1950 in accordance with yet another embodiment of the invention. Structure 1900 is similar to structure 1700, except that once a via is formed through layer 1950, an isotropic

etch process (e.g., chemical or plasma) is employed to form the via through electrode 1910, such that a sloped intersection between an ion conductor 1930 and electrode 1910 is formed.

Figures 21 and 22 illustrate another programmable device 2100, with a reduced electrode/ion conductor interface, in accordance with the present invention. Structure 2100 includes electrodes 2110 and 2120 and an ion conductor 2130, formed on a surface of an insulating material 2140, rather than within a via as discussed above. In this case, the programmable structure is formed by defining an ion conductor 2130 pattern on a surface of insulating material 2140 (e.g., using deposition and etch techniques) and forming electrodes 2110 and 2120, such that the electrodes each contact a portion of the ion conductor. In the case of the illustrated embodiment, the electrodes are formed overlying and in contact with both a portion of the ion conductor and the insulating material. Although the thickness of the layers may be varied in accordance with specific applications of the device, in a preferred embodiment of the invention, the thickness of the ion conductor and electrode films is about 1 nm to about 100 nm. Sub-lithographic lateral dimensions of portions of the device may be obtained by overexposing photoresist used to pattern the portions and/or over etching the film layer.

Figures 23-26 illustrate another embodiment of the invention, where the cross sectional area of the ion conductor/electrode interface is relatively small. Structure 2300, illustrated in Figure 23, includes electrodes 2310 and 2320 and an ion conductor 2330. Structure 2300 is formed in a manner similar to structure 1700, except that the ion conductor material is deposited conformally, using, for example, chemical vapor deposition or physical vapor deposition, into a trench, and the trench is not filled with the ion conductor material.

Structure 2400 is similar to structure 2300, except that an ion conductor 2430 is formed by etching a portion of ion conductor 2330, such that a via 2440 is formed through to electrode 2310. Structure 2500 is similar to structure 2400 and is formed by conformally depositing the ion conductor material as described above and then removing the ion conductor material from a surface of insulating material 2350 prior to depositing electrode 2320 material. Finally, structure 2600 may be formed by selectively deposing the ion conductor 2630 material into only a portion of the trench formed in insulating material 2350 (e.g., using angled deposition and/or shadowing techniques), removing any excess ion conductor material on the surface of insulator 2350, and forming an electrode 2620 overlying the insulator and in contact with ion conductor 2630.

Figures 27 and 28 illustrate yet another embodiment of the invention, where a pillar or wall within a trench is used to reduce a cross-sectional area of the interface between the ion conductor and one or more electrodes. Structure 2700, illustrated in Figure 27, includes electrodes 2710 and 2720 and an ion conductor 2730 formed within an insulating layer 2740. In addition, structure 2700 includes a pillar 2750 of insulating material (e.g., insulating material used to form layer 2740). Structure 2700 may be formed using the shadowed deposition technique discussed above. Structure 2800 is similar to structure 2700 except structure 2800 includes a partial pillar 2850 and an ion conductor 2830, which fills the remaining portion of the formed trench.

Figure 29 illustrates yet another structure 2900 in accordance with the present invention. Structure 2900 includes electrodes 2910 and 2920 and an ion conductor 2930 formed within an insulating layer 2940. Structure 2900 is formed using an anisotropic or a combination of an anisotropic and an isotropic etch processes to form a tapered via. Ion conductor 2930 is then formed within the trench using techniques previously described.

Figures 30-33 illustrate programmable devices in accordance with yet another embodiment of the invention. The structures illustrated in Figures 30-33 include a floating electrode, which facilitates storage of multiple bits of information within a single programmable device.

Structure 3000 includes a first electrode 3010, a second, floating electrode 3020, a third electrode 3030, ion conductor portions 3040 and 3050, which may all be formed on a substrate or wholly or partially formed within a via as described above. Although structure 3000 is illustrated in a vertical configuration, the structure may be formed in a horizontal configuration. In accordance with one aspect of this embodiment, the first and third electrodes are formed of an indifferent electrode material and the second electrode is formed of an oxidizable electrode material. Alternatively, the first and third electrodes may be formed of oxidizable electrode material and the second, floating electrode may be formed of an indifferent electrode material. In either case, the structure includes two "half cells," where each half cell functions as a programmable device described above in connection with Figure 1. Each half cell is preferably configured such that the resistance of one half cell differs from the resistance of the other half cell when both cells are in an erased state.

In the case when floating electrode 3020 is formed of oxidizable electrode material, bits of data may be stored as follows. The overall impedance of structure 3000 is approximately equal to the resistance of portions 3040 and 3050. When no electrodeposit is

formed within either portion, this high resistance state may be represented by the state 00. When a voltage is applied to structure 3000, such that electrode 3030 is positive relative to electrode 3010 and the applied bias is greater than the threshold voltage required to form an electrodeposit in portion 3040, an electrodeposit 3060 will form through conductor portion 3040 from electrode 3010 toward floating electrode 3020 as illustrated in Figure 31. Under this condition, an electrodeposit will not form within conductor portion 3050 because portion 3050 is under a reverse bias condition and thus will not support growth of an electrodeposit. The growth of the electrodeposit will change the impedance of portion 3040 from $Z_1$ to $Z_1$', thus changing the overall impedance of structure 3000, which may be represented by the state 01. The current level used to form electrodeposit 3060 should be selected such that it is sufficiently low, allowing the electrodeposit to be dissolved upon application of a sufficient reverse bias. A third state may be formed by reversing the polarity of the applied bias across electrodes 3010 and 3030, such that most of the voltage drop occurs across the high resistance ion conductor portion 3050 and formation of an electrodeposit 3070 begins, as illustrated in Figure 32, without causing electrodeposit 3060 to dissolve. The impedance of portion 3050 changes from $Z_2$ to $Z_2$', and the overall impedance of structure 3000 is $Z_1$' plus $Z_2$', which may be represented by the state 11. Once both half cells are in the write state, electrodeposit 3060 and/or 3070 may be dissolved by applying a sufficient bias across one or both of the half cells. Electrodeposit 3070 can be erased, for example, by sufficiently negatively biasing electrode 3030 with respect to electrode 3010, which may be represented by a state 00. The four possible states, along with the current limit used to form the state, are represented in table 1 below.

| Seq # | Polarity | Current limit | Z half-cell 1 | Z half-cell 2 | State/value |
|---|---|---|---|---|---|
| 1 | Sub-threshold | Zero | $Z_1$ | $Z_2$ | 00 |
| 2 | Upper + Lower – | Low | $Z_1$' | $Z_2$ | 01 |
| 3 | Upper – Lower + | Low | $Z_1$' | $Z_2$' | 11 |
| 4 | Upper – Lower + | High | $Z_1$ | $Z_2$' | 10 |

Table 1

Structure 3000 can be changed to 11 from state 10 by applying a low current limit bias to grow electrodeposit 3050 in portion 3040. Similarly, structure 3000 can be changed from state 11 to state 01 by dissolving electrodeposit 3070 by applying a relatively high current limit bias such that upper electrode 3030 is positive with respect to lower electrode 3010. Finally, structure 3000 can be returned to state 00 using a short current pulse to thermally dissolve electrodeposit 3060, using a current which is high enough to cause localized heating of the electrodeposit. This will increase the metal concentration in the half-cell but this excess metal can be removed electrically from the cell by plating it back onto the floating electrode. This sequence is summarized in table 2 below.

| Seq # | Polarity | Current limit | Z half-cell 1 | Z half-cell 2 | State/value |
|---|---|---|---|---|---|
| 4 | Existing state | - | $Z_1$ | $Z_2$' | 10 |
| 5 | Upper + Lower – | Low | $Z_1$' | $Z_2$' | 11 |
| 6 | Upper + Lower – | High | $Z_1$' | $Z_2$ | 01 |
| 7 | Upper + Lower – | Thermal | $Z_1$ | $Z_2$ | 00 |

Table 2

Other write and erase sequences are also possible (as are other definitions of the various states represented by the half-cell impedances). For example, it is possible to go from state 00 to either state 01 or state 10, depending on the write polarity chosen. Similarly, it is possible to go from state 11 to either state 10 or state 01. It is also possible to go from state 11 to state 00 by the application of a current pulse (in either direction) which is high and short enough to thermally dissolve the electrodeposits in both half-cells simultaneously.

In addition to storing information in digital form, structure 3000 can also be used as a noise-tolerant, low energy anti-fuse element for use in field programmable gate arrays (FPGAs) and field configurable circuits and systems. Most physical anti-fuse technologies require large currents and voltages to make a permanent connection. The need for such high energy state-switching stimuli is generally considered to be somewhat beneficial as this reduces the likelihood of the anti-fuse accidentally forming a connection in electrically noisy situations. However, the use of high voltages and large currents on chip represent a

significant problem as all components in the programming circuits are typically sized accordingly and the high energy consumption reduces battery life in portable systems.

Figures 34-38 illustrate structures in accordance with another embodiment of the invention in which multiple programmable devices include a common electrode (e.g., the devices share a common anode or cathode). Forming structures in which multiple structures share a common electrode is advantageous because such structures allow a higher density of cells to be formed on a given substrate surface area.

Figures 34 and 35 illustrate a structure 3400, having a horizontal configuration and a common electrode. Structure 3400 includes an electrical connector 3410 coupled to a common surface electrode 3420, electrodes 3430 and 3440, and ion conductor portions 3450 and 3460 overlying an insulating layer 3470. Structure 3400 may be used to form word and bit lines as described above by forming a row of electrodes (e.g., anodes) coupled to conductor 3410, and columns of oppositely bias electrodes (e.g., cathodes) running perpendicular to electrodes 3420. A conductive plug, formed of any suitably conducting material, can be used to electrically couple electrode 3420 to conductor 3410. Although illustrated with a horizontal configuration, common electrode structures in accordance with this embodiment may be formed using structures having a vertical configuration as described herein.

Figures 36 and 37 illustrate additional structures 3600 and 3700 having a common electrode shared between two or more devices. Structures 3600 and 3700 include a common electrode, electrodes 3620 and 3625, ion conductors 3630, 3635 and 3730, 3735 respectively, and insulating layers 3640 and 3650. Structures 3600 and 3700 may be formed using techniques described above in connection with Figures 24 and 25—e.g., by conformally depositing ion conductor material within a trench of an insulating layer. In accordance with another embodiment of the invention, directional deposition may be used to form a structure similar to structure 2600. Structures 3600 and 3700 each include two programmable devices including common electrode 3610, an ion conductor (e.g., conductor 3635), and another electrode (e.g., electrode 3625). Dielectric material 3650 is an insulating material that does not interfere with surface electrodeposit growth, such as silicon oxides, silicon nitrides, and the like.

Figure 38 illustrates a structure 3800 including multiple programmable devices 3802-3816 formed about a common electrode 3820. Each of the devices 3802-3816 may be formed using the method described above in connection with Figure 30. In the embodiment

illustrated in Figure 38, each of electrodes 3830-3836 and 3838-3844 may be coupled together in a direction perpendicular to the direction of common electrode 3820, such that electrode 3820 forms a bit line and electrodes 3830-3836 and electrodes 3838-3844 form word lines. Structure 3800 may operate and be programmed in a manner similar to structure 3000 described above.

In accordance with other embodiments of the present invention, a programmable structure or device stores information by storing a charge as opposed to growing an electrodeposit. A capacitance of a structure or device is altered by applying a bias across electrodes of the device such that positively charged ions migrate toward one of the electrodes. If the applied bias is less that a write threshold voltage, no short will form between the electrodes. Capacitance of the structure changes as a result of the ion migration. When the applied bias is removed, the metal ions tend to diffuse away from the electrode or a barrier proximate the electrode. However, an interface between an ion conductor and a barrier is generally imperfect and includes defects capable of trapping ions. Thus, at least a portion of ions remain at or proximate an interface between a barrier and an ion conductor. If a write voltage is reversed, the ions may suitably be dispersed away from the interface.

A programmable structure in accordance with the present invention may be used in many applications which would otherwise utilize traditional technologies such as EEPROM, FLASH or DRAM. Advantages provided by the present invention over present memory techniques include, among other things, lower production cost and the ability to use flexible fabrication techniques which are easily adaptable to a variety of applications. The programmable structures of the present invention are especially advantageous in applications where cost is the primary concern, such as smart cards and electronic inventory tags. Also, an ability to form the memory directly on a plastic card is a major advantage in these applications as this is generally not possible with other forms of semiconductor memories.

Further, in accordance with the programmable structures of the present invention, memory elements may be scaled to less than a few square microns in size, the active portion of the device being less than on micron. This provides a significant advantage over traditional semiconductor technologies in which each device and its associated interconnect can take up several tens of square microns.

Programmable structures and devices and system including the programmable structures described herein are advantageous because the programmable structures require relatively little internal voltage to perform write and erase functions, require relatively little

current to perform the write and erase functions, are relatively fast (both write and read operations), require little to no refresh (even for "volatile" memory applications), can be formed in high-density arrays, are relatively inexpensive to manufacture, are robust and shock resistant, and do not require a monocrystalline starting material and can therefore be added to other electronic circuitry.

Although the present invention is set forth herein in the context of the appended drawing figures, it should be appreciated that the invention is not limited to the specific form shown. For example, while the programmable structure is conveniently described above in connection with programmable memory devices, the invention is not so limited; the structure of the present invention may additionally or alternatively be employed as programmable active or passive devices within a microelectronic circuit. Furthermore, although only some of the devices are illustrated as including buffer, barrier, or transistor components, any of these components may be added to the devices of the present invention. Various other modifications, variations, and enhancements in the design and arrangement of the method and apparatus set forth herein, may be made without departing from the spirit and scope of the present invention as set forth in the appended claims.

## CLAIMS

I claim:

1. A microelectronic programmable structure comprising:
an ion conductor comprising oxygen and conductive material;
an oxidizable electrode proximate the ion conductor; and
an indifferent electrode proximate the ion conductor.

2. The microelectronic programmable structure of claim 1, wherein the ion conductor further comprises a material selected from the group consisting of sulfur, selenium, and tellurium.

3. The microelectronic programmable structure of claim 1, wherein the ion conductor comprises an oxide material selected from the group consisting of $GeO_2$, $As_2O_3$, $Ag_2O$, $Cu_{(1,2)}O$, and $SiO_2$.

4. The microelectronic programmable structure of claim 1, wherein the ion conductor comprises a material selected from the group consisting of $Ge_xS_{1-x}$, $As_xS_{1-x}$, $GexSe_{1-x}$, $As_xSe_{1-x}$, $Ge_xTe_{1-x}$, and $As_xTe_{1-x}$.

5. The microelectronic programmable structure of claim 1, wherein the conductive material comprises a material selected from the group consisting of silver and copper.

6. The microelectronic programmable structure of claim 1, further comprising a barrier layer between the oxidizable electrode and the indifferent electrode.

7. A microelectronic programmable structure comprising:
an ion conductor comprising a first region having a first resistance and a second region having a second resistance, wherein the first resistance and the second resistance differ;
an oxidizable electrode proximate the ion conductor; and

an indifferent electrode proximate the ion conductor.

8. The microelectronic programmable structure of claim 7, wherein the first region comprises a conductive material and the second region comprises a chalcogenide material.

9 The microelectronic programmable structure of claim 7, wherein the first region comprises a conductive material and the second region comprises an oxide material.

10 The microelectronic programmable structure of claim 7, wherein the first region comprises a conductive material and the second region comprises a polymeric material.

11. The microelectronic programmable structure of claim 7, wherein the first region comprises a material selected from the group consisting of $Ag_2S$, $Ag_2Se$, and $Ag_2Te$.

12. The microelectronic programmable structure of claim 7, wherein the second region comprises a material selected from the group consisting of $Ge_xSe_{1-x}$, $Ge_xS_{1-x}$, $Ge_xTe_{1-x}$, $As_xSe_{1-x}$, $As_xS_{1-x}$, $As_xTe_{1-x}$, $SiO_x$, $GeO_x$, and $Ag_2O$.

13. The microelectronic programmable structure of claim 7, wherein the first region is dispersed within the second region.

14. The microelectronic programmable structure of claim 7, wherein the first region and the second region form adjacent layers of the structure.

15. The microelectronic programmable structure of claim 7, wherein the second region is formed about a perimeter of the first region.

16. A method of programming a microelectronic device, the method comprising the steps of:

providing a programmable structure comprising an ion conductor and a conductive material dispersed within the ion conductor; and

applying a pulse of energy across the ion conductor, the pulse of energy having a voltage greater than the reduction/oxidation potential of the structure, wherein the energy is lower than the amount of energy required to perform a permanent write or erase operation.

17. The method of claim 16, further comprising a read operation, wherein an amount of energy supplied to the structure during the read operation is sufficient to restore a write state of the structure.

18. A method of altering a read/write threshold potential of a programmable structure, the method comprising the steps of:

providing a programmable structure comprising an ion conductor and a conductive material dispersed within the ion conductor; and

altering an amount of conductive material dispersed within the ion conductor.

19. The method of claim 18, wherein the altering step includes supplying a sufficient bias across the ion conductor to alter an amount of conductive material within the ion conductor.

20. A microelectronic programmable structure comprising:

an ion conductor;

an oxidizable electrode proximate the ion conductor;

an indifferent electrode proximate the ion conductor; and

a resistive barrier between the indifferent electrode and the ion conductor.

21. The microelectronic programmable structure of claim 20, wherein the resistive barrier comprises conductive material.

22. The microelectronic programmable structure of claim 20, wherein the resistive barrier comprises a material selected from the group consisting of a gas-filled region, a vacuum, a porous oxide film, and a chalcogenide material.

23. The microelectronic programmable structure of claim 20, wherein the resistive barrier comprises ion conductor material.

24. A method of reading information stored in a programmable device, the method comprising the steps of:

providing a programmable device with an unknown state;

applying a voltage across the programmable device;

producing a temperature compensation signal;

detecting a current passing through the programmable device; and

comparing the temperature compensation signal to the current to determine the state of the device.

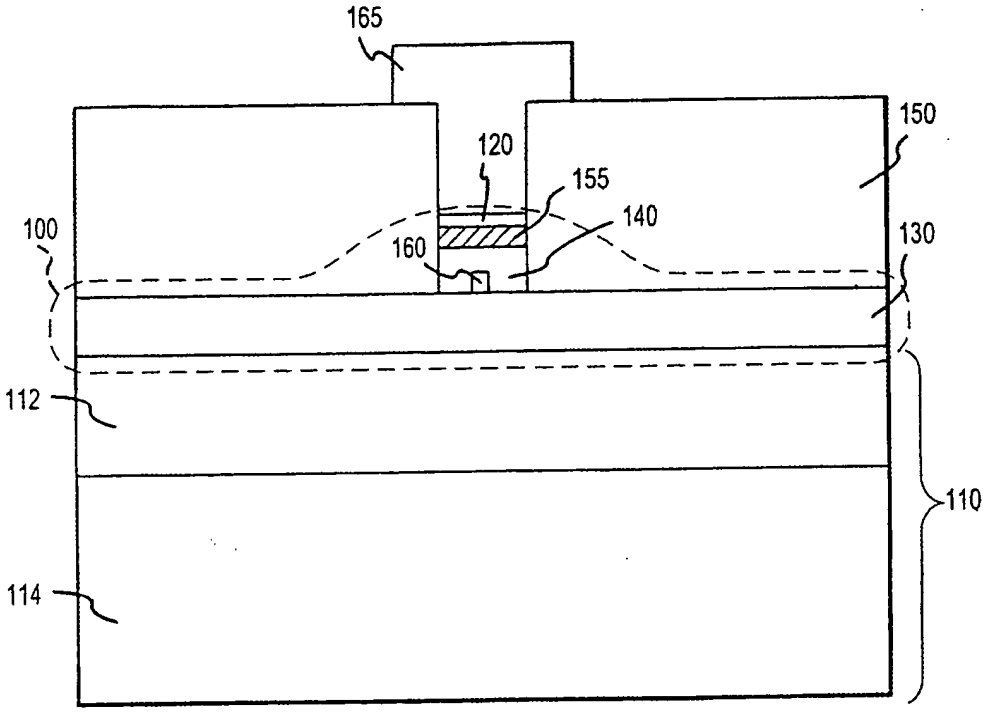



FIG.1

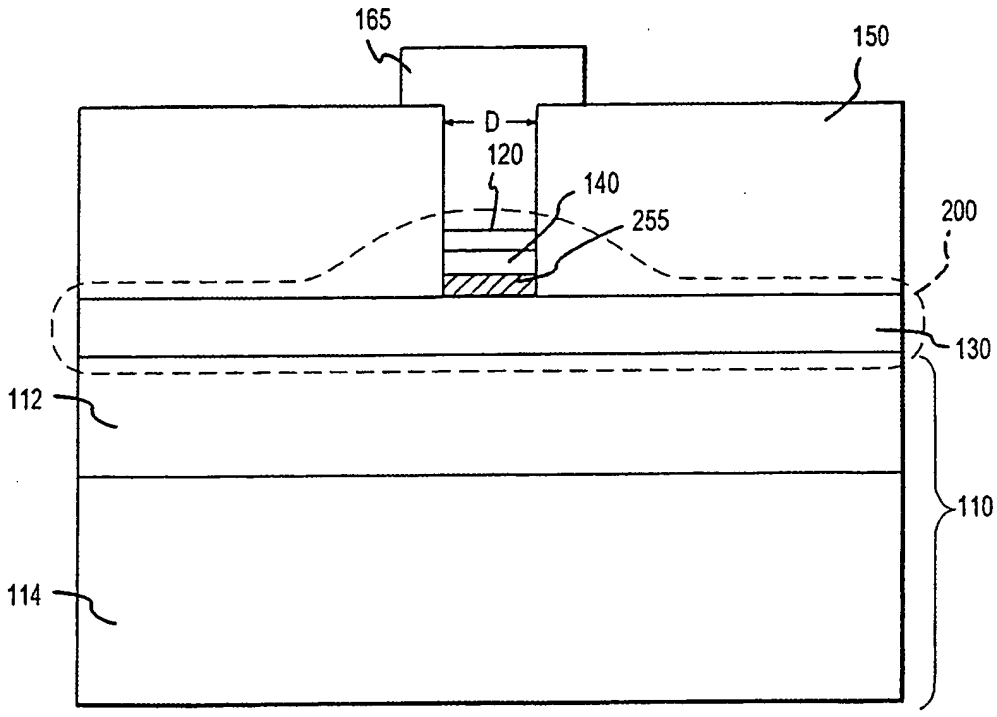



FIG.2

s) and mixtures of these, and Cu as a substitute for Ag i
y low resistivity dispersed phase in a continuous or nea
ase, the combination of which is capable of supporting i
same effect. For example, $Ag_2Se$ dispersed in AgI or ir
ı as poly(ethylene oxide) can also be used. The high re
aterial which is not usually considered to be a "good" ioı
s $SiO_2$, $GeO_2$, or $Ag_2O$, as long as the thickness of this
:onducting regions is small (less than 1 nm or so). Sucl
: of supporting ion transport under high local field. The
:presentation of a generalized phase-separated electrol
guration.

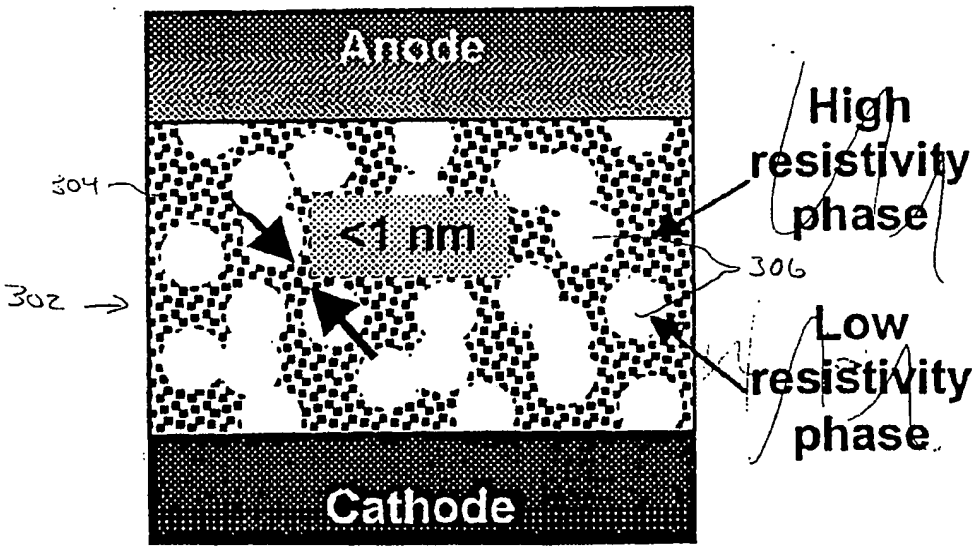



FIG. 3

ıctures, in which the low resistivity phase is laterally spli
'ers of [redacted] material, will also behave in a
on of [redacted]

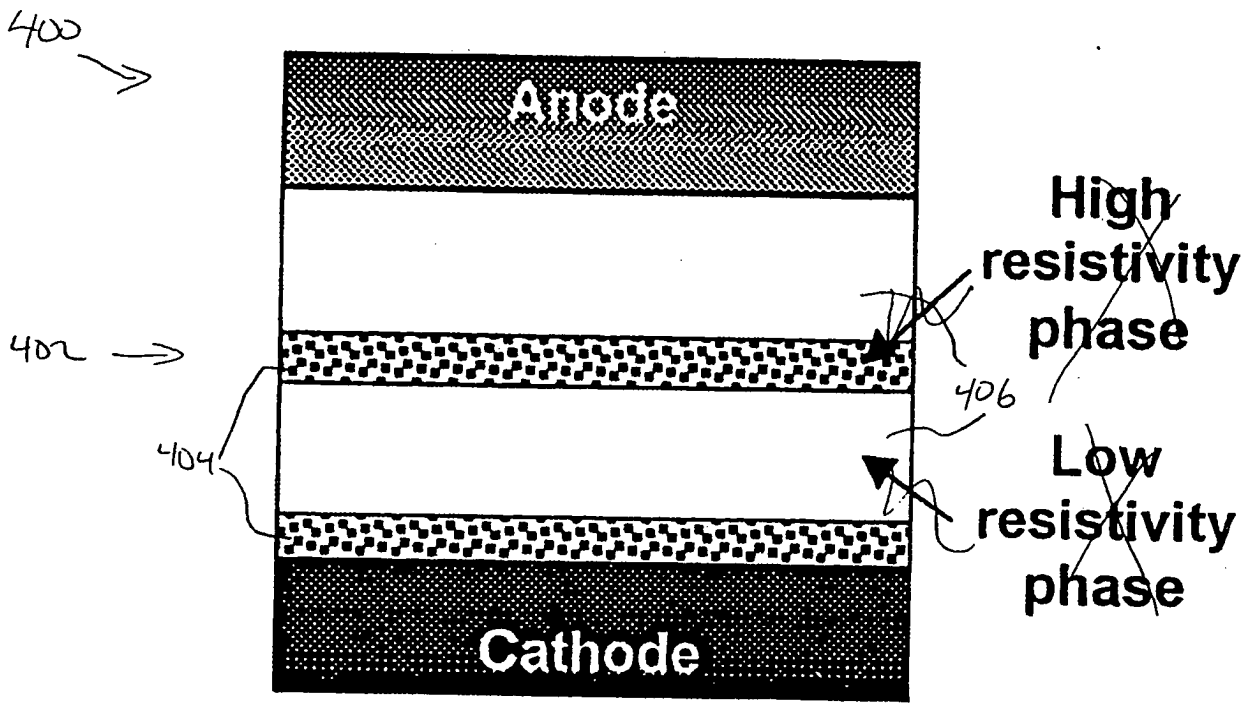



Fig. 4

) possible to obtain a similar effect using a collection of particles of the lo
:y phase that have been coated with the high resistivity material in contac
)elow.

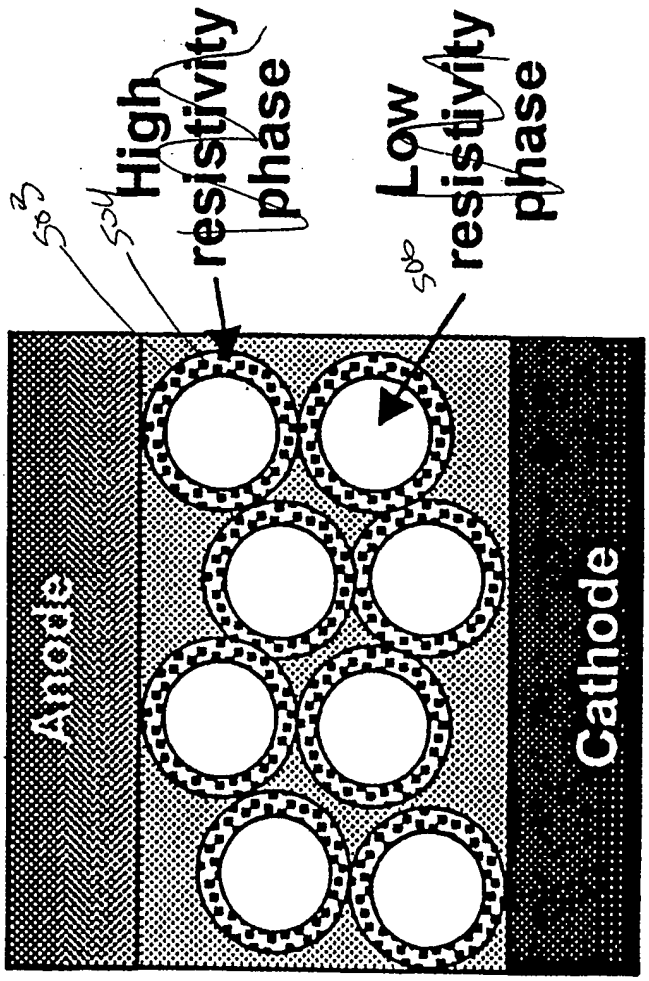

High resistivity phase
Low resistivity phase
Anode
Cathode
504
506
508
500
502

Fig. 5

below.

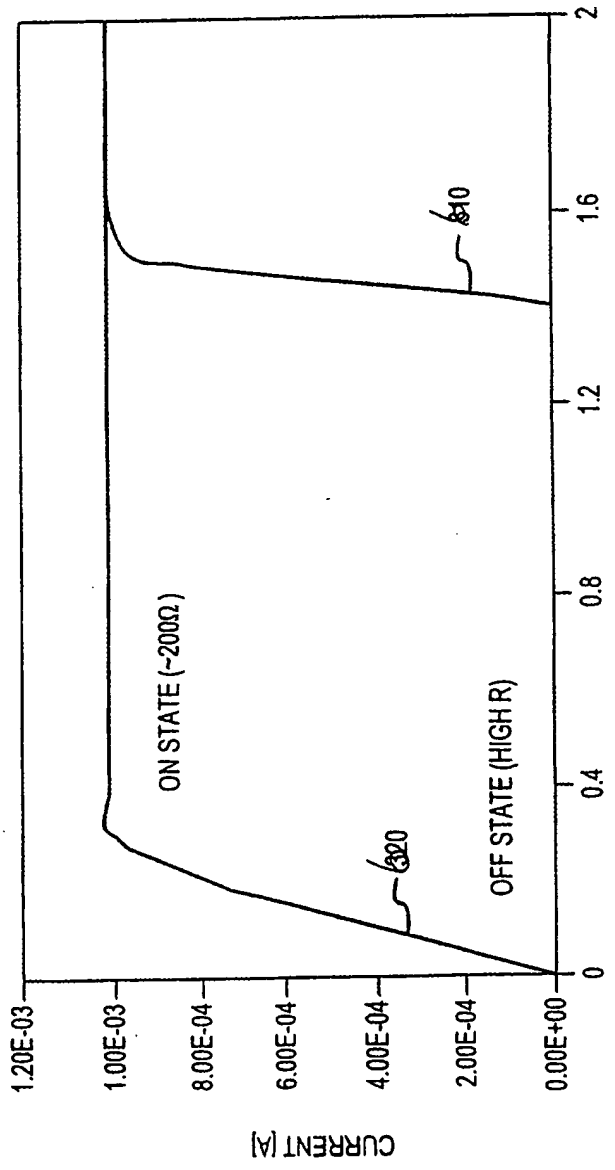

CURRENT [A]
1.20E-03
1.00E-03
8.00E-04
6.00E-04
4.00E-04
2.00E-04
0.00E+00
0
0.4
0.8
1.2
1.6
2
VOLTAGE [+V]
ON STATE (~200Ω)
OFF STATE (HIGH R)
320
310

FIG. 3

lightly doped starting glass (Ge-S or Ge-Se) or a variety of other silver-lean materials, including those glasses which have an inherently low silver solubility. This layer will separate the silver rich electrolyte from the cathode and will help to reduce silver build-up near the electrode during processing and device operation. In this way, the write threshold will be maximized and maintained. An example of a write operation on a PMCm device which utilizes a silver saturated sulfur-rich Ge-S starting glass is shown below (current vs. voltage and resistance vs. voltage for a 1 μA programming current). A layer of relatively low silver content, less than 10 nm thick, has been left between the cathode and the Ag-saturated electrolyte so that the write voltage lies around 320 mV. Note that this layer could be deposited separately from the Ag-rich electrolyte or can be formed, as it was in the case below, by stopping the silver (photo)diffusion before the metal penetrates the entire film thickness.

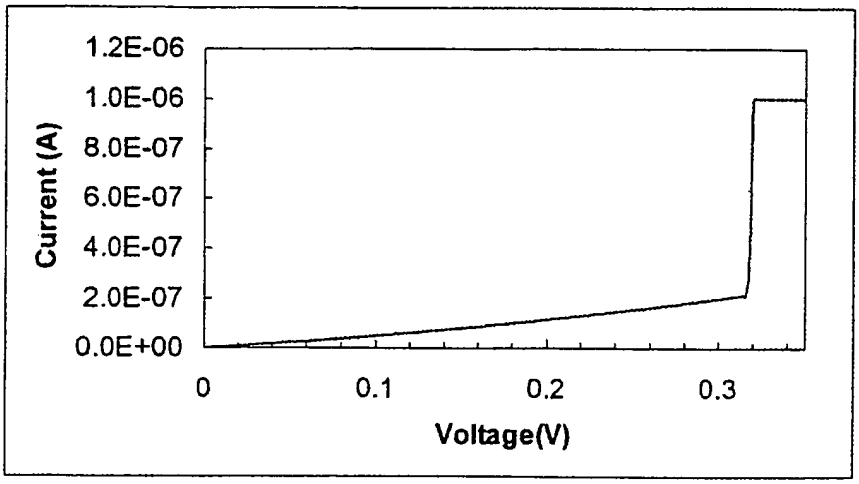



Fig. 7

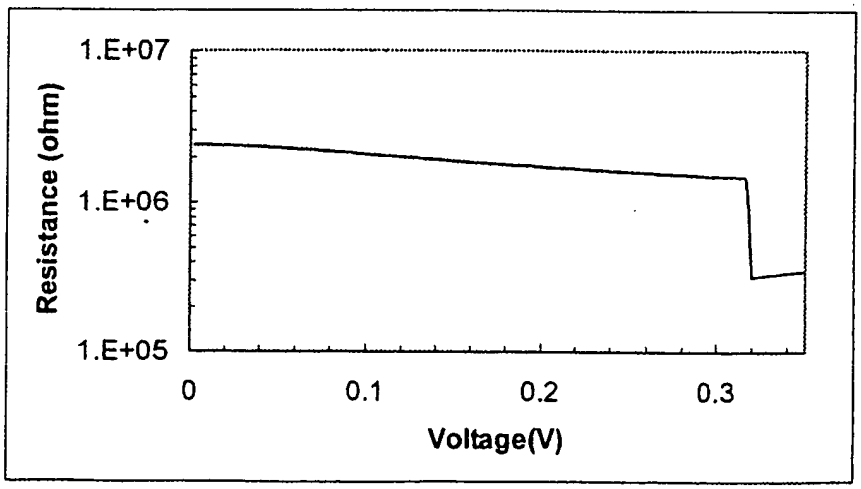



Fig. 8

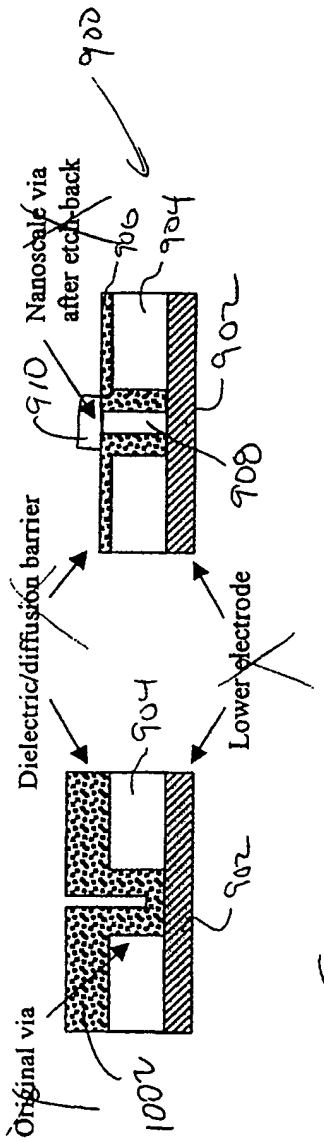
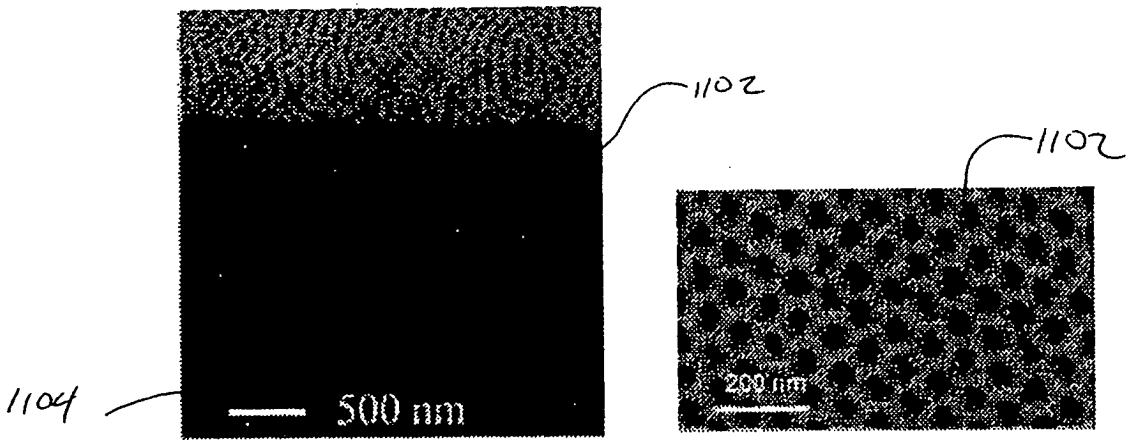

900
Nanoscale via after etch-back
906
904
902
910
908
Dielectric/diffusion barrier
Lower electrode
904
902
Original via
1002

Fig. 9

Fig. 10




Cross-section of porous alumina.

Top view of nanopores in alumina.

FIG. 11

FIG. 12

Alternatively, a layer such as that shown above (preferably a thinner version) could be used as an etch mask for the solid electrolyte during anisotropic etching to pattern the

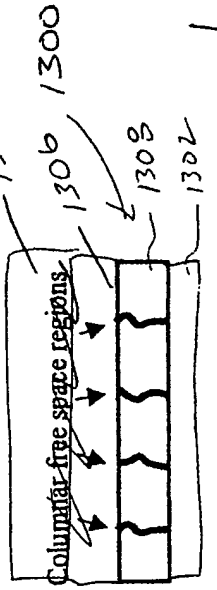



Fig. 13

Candidates for such materials are thin (e.g. a few nm) amorphous films of oxides and nitrides (e.g., $SiO_2$, $GeO_2$, $Si_3N_4$) and semiconductors (Si, Ge) and polycrystalline films of oxides, nitrides, and semiconductors. This layer would typically be placed between the solid electrolyte and the cathode.

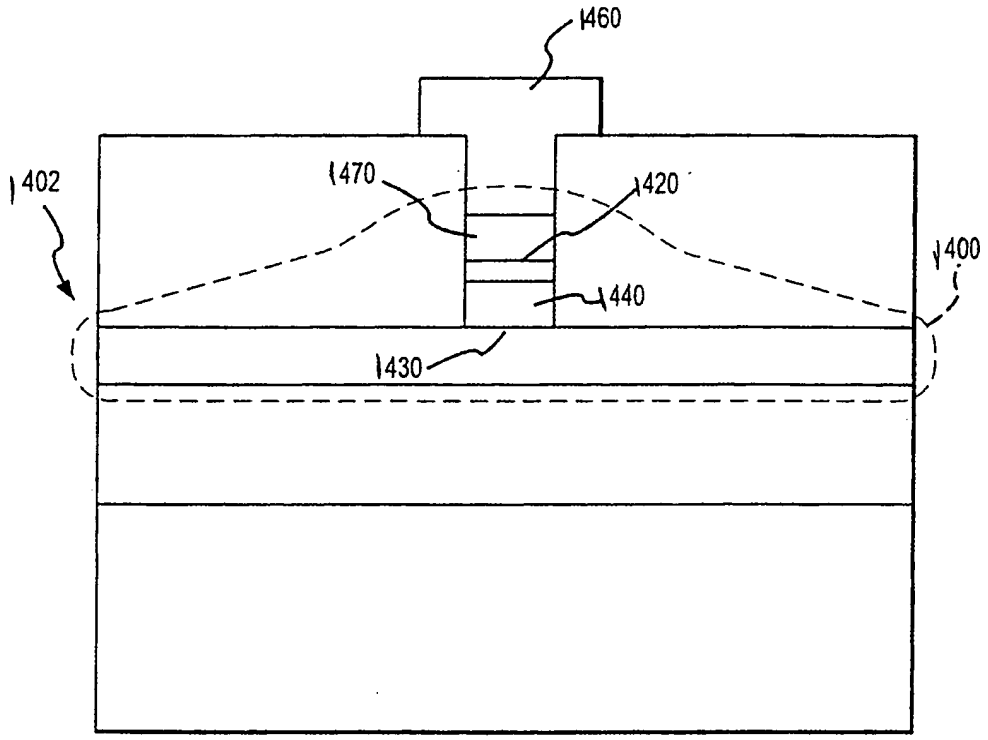



FIG. 4

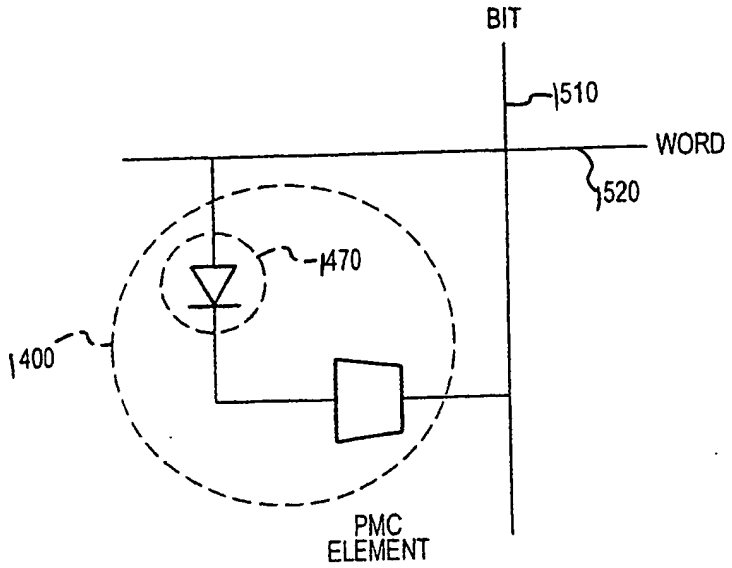



FIG.5 15

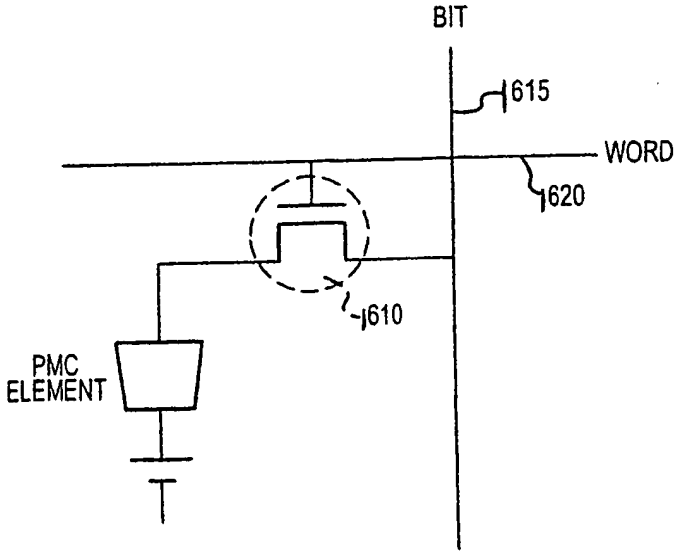



FIG.6 16

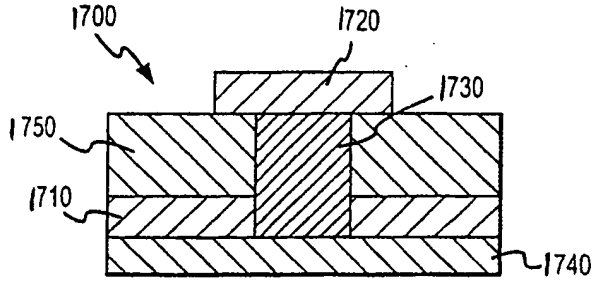



FIG. 17

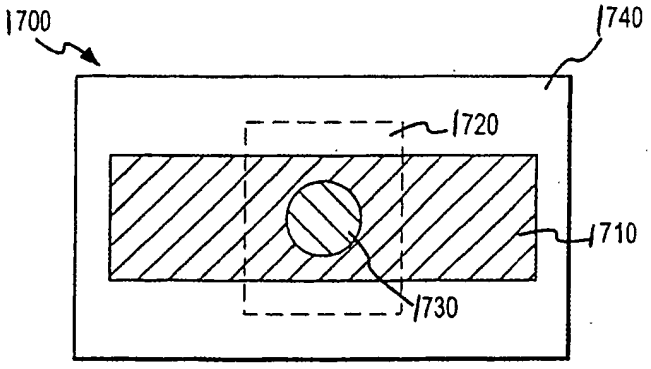



FIG. 18

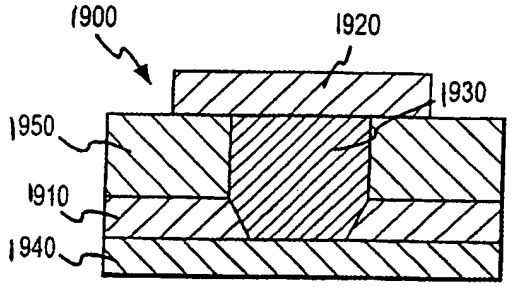



FIG. 9 19

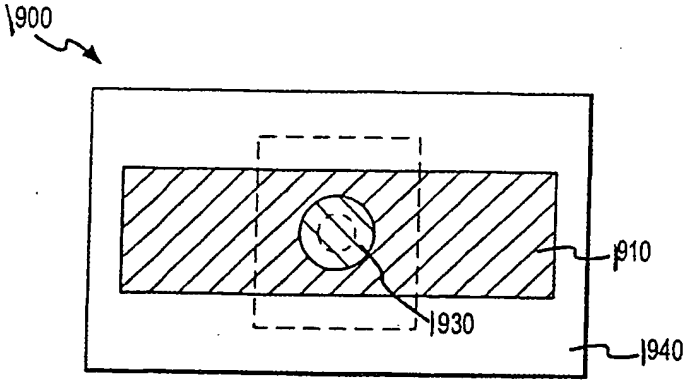



FIG. 10 20

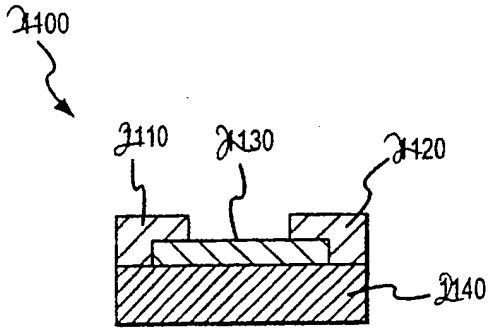



FIG. 11 21

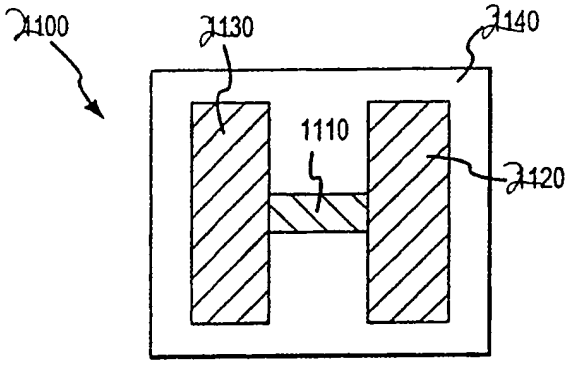



FIG. 12 22

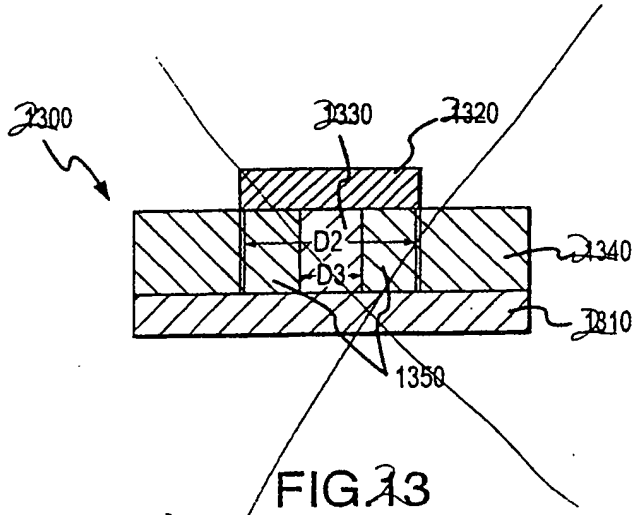



FIG. 13

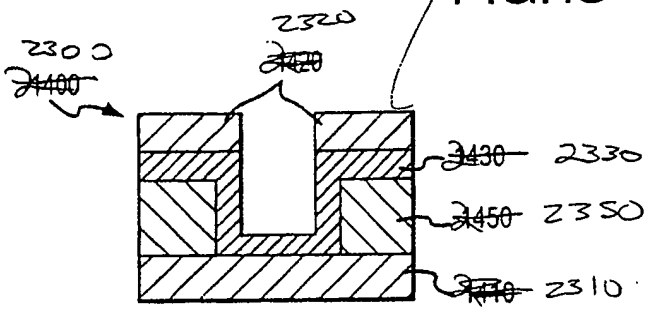



FIG. 14 23

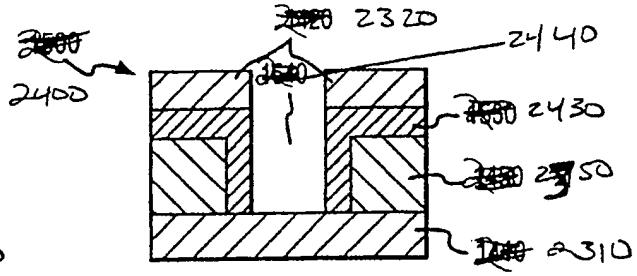



FIG. 15 24

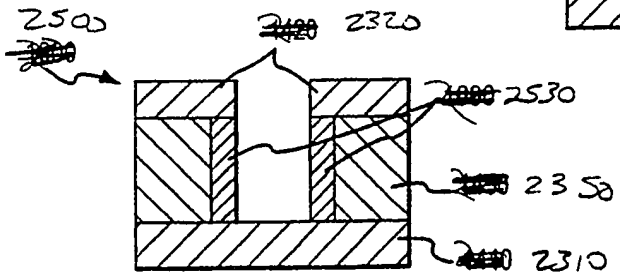



FIG. 16 25

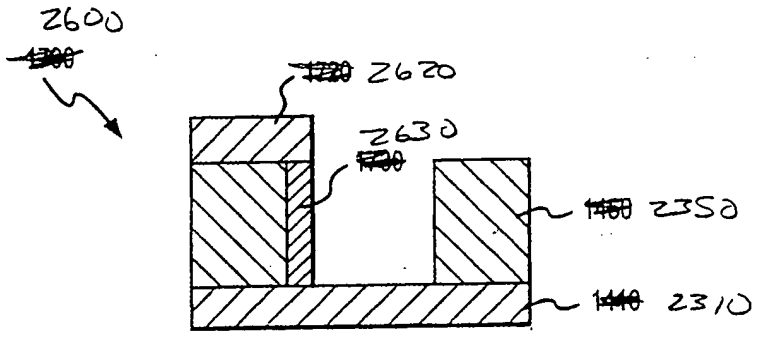



FIG. 17 26

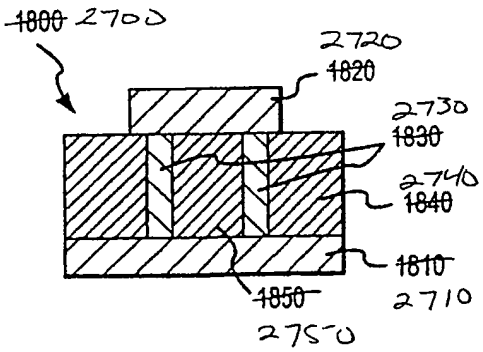



FIG. 18 27

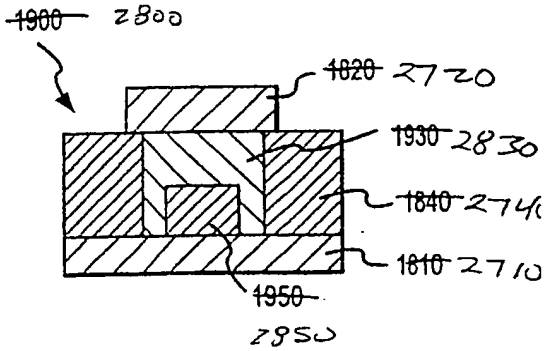



FIG. 19 28

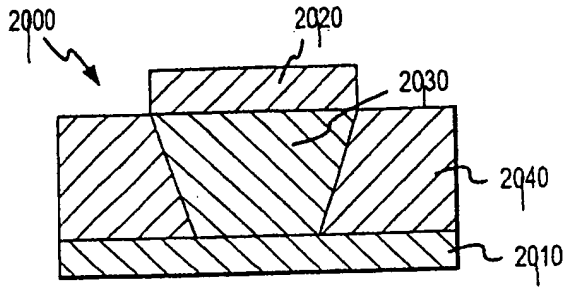



FIG.20 29

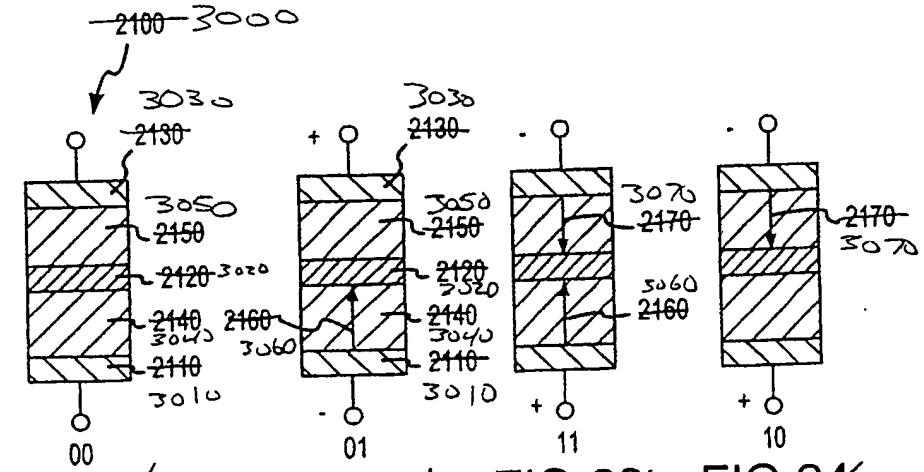



FIG.21 30 FIG.22 31 FIG.23 32 FIG.24 33

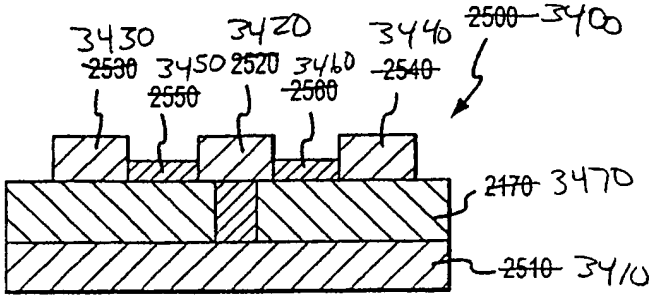



FIG.25 34

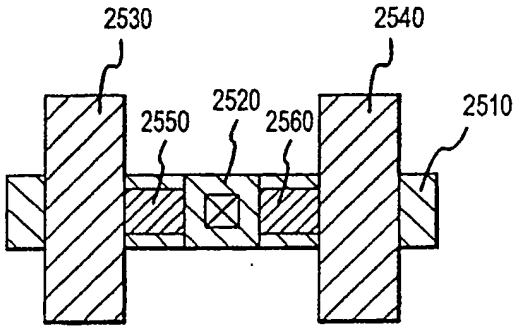
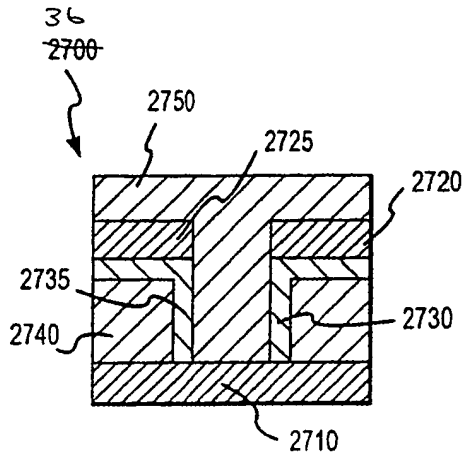



FIG.26 35

"28" → "37"
"27" → "36"




"27" → "36"

FIG. 27 36

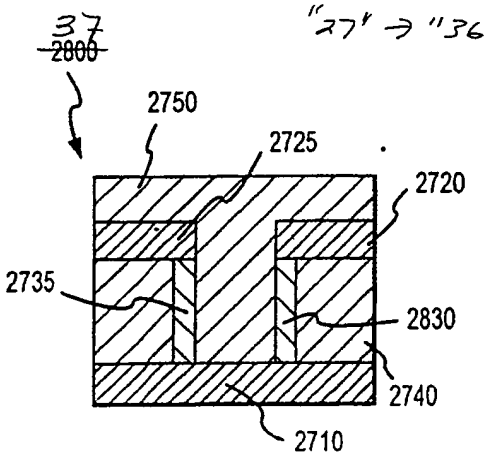
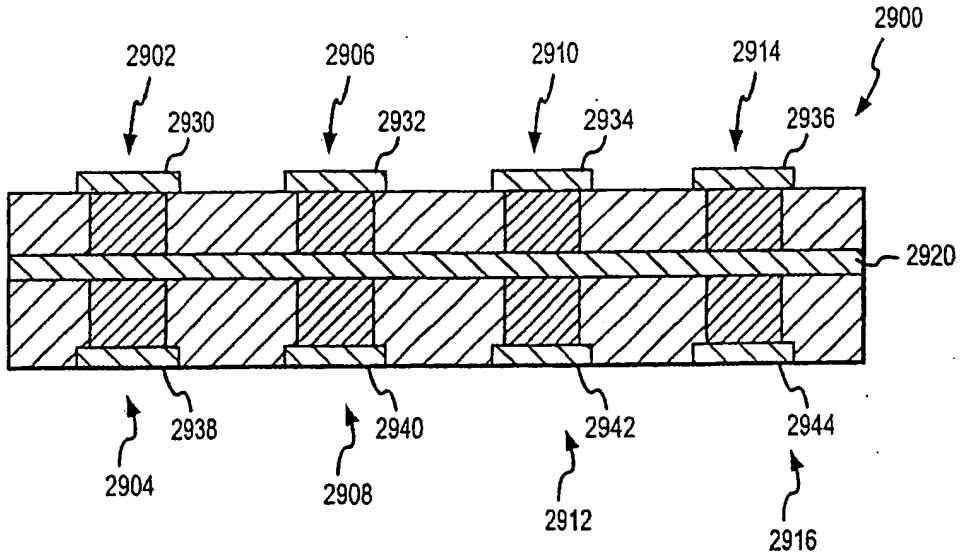



FIG. 28 37




"129" → "38"

FIG. 29 38

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| 60/367,582 | 20 March 2002 (20.03.2002) | US |

(71) Applicant *(for all designated States except US)*: **AXON TECHNOLOGIES CORPORATION** [US/US]; 7702 East Doubletree Ranch Road, Suite 300, Scottsdale, AZ 85258 (US).

(72) Inventor; and

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(74) Agent: **PILLOTE, Cynthia, L.**; Snell & Wilmer L.L.P., One Arizona Center, 400 East Van Buren, Phoenix, AZ 85004-2202 (US).

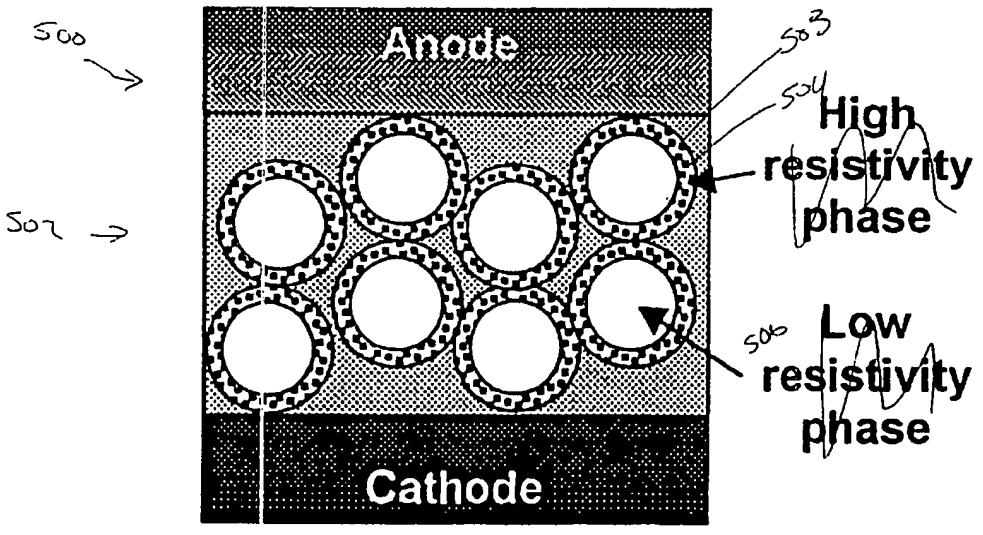
(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, OM, PH, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

**Published:**
--- *with international search report*

*[Continued on next page]*

(54) Title: PROGRAMMABLE MICROELECTRONIC DEVICE, STRUCTURE, AND SYSTEM, AND METHOD OF FORMING THE SAME




(57) Abstract: A microelectronic programmable structure suitable for storing information and a method of forming and programming the structure are disclosed. The programmable structure generally includes an ion conductor and a plurality of electrodes. Electrical properties of the structure may be altered by applying energy to the structure, and thus information may be stored using the structure.

WO 03/032392 A3

**(88) Date of publication of the international search report:**
20 November 2003

*For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.*

# INTERNATIONAL SEARCH REPORT

International Application No
PC., .S 02/32099

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 G11C11/34 G11C11/56 H01L45/00

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 G11C H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data, PAJ, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

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| X | WO 00 48196 A (KOZICKI MICHAEL N ;UNIV ARIZONA (US)) 17 August 2000 (2000-08-17) page 5, line 10 -page 11, line 27 | 18,19 |
| Y | | 1-6,8-15 |
| A | | 17 |
| | --- | |
| | -/-- | |

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

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"&" document member of the same patent family

| Date of the actual completion of the International search | Date of mailing of the International search report |
|---|---|
| 10 March 2003 | 13.08.2003 |

| Name and mailing address of the ISA | Authorized officer |
|---|---|
| European Patent Office, P.B. 5818 Patentlaan 2<br>NL - 2280 HV Rijswijk<br>Tel. (+31-70) 340-2040, Tx. 31 651 epo nl,<br>Fax: (+31-70) 340-3016 | Colling, P |

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# INTERNATIONAL SEARCH REPORT

International Application No
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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

| Category ° | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|---|---|---|
| X | KOZICKI M N ET AL: "Nanoscale effects in devices based on chalcogenide solid solutions" THIRD INTERNATIONAL WORKSHOP ON SURFACES AND INTERFACES IN MESOSCOPIC DEVICES - (SIMD'99), MAUI, HI, USA, 6-10 DEC. 1999, vol. 27, no. 5-6, pages 485-488, XP002233827 Superlattices and Microstructures, 2000, Academic Press, UK ISSN: 0749-6036 | 7,18,19 |
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Form PCT/ISA/210 (continuation of second sheet) (July 1992)

# INTERNATIONAL SEARCH REPORT

Ir tional application No.
PCT/US 02/32099

**Box I Observations where certain claims were found unsearchable (Continuation of item 1 of first sheet)**

This International Search Report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the International Application that do not comply with the prescribed requirements to such an extent that no meaningful International Search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

**Box II Observations where unity of invention is lacking (Continuation of item 2 of first sheet)**

This International Searching Authority found multiple inventions in this international application, as follows:

see additional sheet

1. ☐ As all required additional search fees were timely paid by the applicant, this International Search Report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying an additional fee, this Authority did not invite payment of any additional fee.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this International Search Report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this International Search Report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:
1-19

**Remark on Protest**

☒ The additional search fees were accompanied by the applicant's protest.

☐ No protest accompanied the payment of additional search fees.

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

1. Claims: 1-19

Programmable microelectronic device comprising ion conductor material between electrodes.

2. Claims: 20-23

Programmable microelectronic device comprising ion conductor material between electrodes with resistive barrier between indifferent electrode and ion conductor

3. Claim : 24

Reading method for programmable microelectronic device using temperature compensation

# INTERNATIONAL SEARCH REPORT

International Application No
PC., .S 02/32099

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